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Faults Identification in Digital Counter Using Naïve-Bayes' Algorithm

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***Abstract*:-**This paper elaborates on the implementation of the Naïve Bayes Algorithm to identify the faults occurrence in the digital counter circuits. The digital counters are circuits utilized to count the values in increasing order, decreasing order, or both directions. The digital counters find applications in real time from simple wristwatches to the industrial conveyor belt that is automated based on timings. The fault happening in the digital counter circuit is to be identified using Fault detection methods such as modular redundancy methods and error detection methods. With the advent of Artificial Intelligence algorithms, the identification of faults and errors in circuits is attained rapid manner. Though there are several machine learning algorithms such as Decision trees, Random Forest, K-Nearest Neighbor, and Support Vector Machines, the naïve Bayes algorithm is an easy and efficient algorithm to identify the errors in the circuits. This work concentrates on the naïve Bayes algorithm by developing the HDL code to predict the faults in the counter circuits. The proposed HDL code is validated for parameters namely power, area, and timing using the EDA tools.

Keywords: *Fault Analysis, Naïve Bayes Algorithm, Counters, Electronic Design Automation Tools*

I Introduction

In digital system design, the counter circuit is a digital circuit that keeps track of the number of events occurring as per the count required. The counter circuit is the common component in any automated circuit used in real-time. The fault occurrence in digital circuits can degrade the overall performance of the system either temporarily or permanently. The need for fault analysis arises to identify, rectify, and eradicate such faults in real-time digital applications.

Several fault identification techniques can be used with the digital logic namely Triple Modular Redundancy, 5 Modular Redundancy, and N-modular Redundancy, and consume a high area in the design of these redundancy-based fault analyzing circuits. To overcome this, the faults in the digital circuits are identified using Artificial Intelligence algorithms namely the Decision tree method, Random forest method,K-nearest neighbor, and Support Vector Machines. Though many algorithms are available to analyze the faults, the Naïve Bayes algorithm is easy and simple to efficiently identify the faulty instances in the circuits.

The k-nearest neighbors (KNN) technique can be used to locate the problem, and the LSTM algorithm can be used to anticipate the preceding value of the power inverter input [1].Artificial intelligence is used to forecast the power system characteristics to eliminate unexpected current flow, power outages, and leakage of amperes in industrial applications [2]. The machine learning-based technique can be used to assess line faults and changingimpedance issues in inverter-generators linked to transmission lines [3].In the micro-grid supplied generator based on inverter, the problematic phases are retrieved using the Pearson correlation coefficient-based approach [4]. In real-time power converters, the fault occurrence of a single-phase value can be accomplished using Classification & Regression Tree (CART) approach [5]. The teenager-kaiser energy operator algorithm, which has a low computational time and complexity, can be used to investigate DC faults [6].

The Naive Bayes algorithm is used to identify, classify, or predict the faults with the given dataset [7]. The real-time application-based Naïve Bayes algorithm is challenging to implement as it consists of probability functions [8]. The FPGA-based Naïve Bayes algorithm demands the compensatory approach to accurately derive the fault in the circuits. The HDL code for the probability function is not synthesizable in real time [9]. The need for an alternate approach may increase the size of the circuit under test.

This paper proposes the Naïve Bayes algorithm implementable using the FPGA device to identify the fault occurrence in the digital counter circuit. The synthesizable code for the proposed method is developed in HDL and the IC layout is presented for the proposed method using the VLSI EDA tools.

II. The Proposed Method: Naïve Bayes algorithm based Fault analysis for the counter circuit

The proposed Naïve Bayes algorithm-based fault analysis for digital counter circuits investigates the error occurrence in the counter circuit in digital design. The design for the fault analysis of the counter consists of two counter circuits of 2^8-bit resolution. One of the counters is the counter circuit under test referred to as the "Valid Counter" and the other counter identifies the fault referred to as the "Fault Counter". The Valid counter is the counter used to generate the correct and errorless counting output and the fault counter is the circuit that produces the faulty output of the counter circuit. These two counters are generated simultaneously and the outputs of the counters are analysed for faults.

The counter outputs are fed into the Naïve Bayes algorithm block with the comparator as shown in Figure 1. This work uses the Naïve Bayes algorithm to predict the faults in the digital counter circuit. In general, Naïve Bayes algorithm is a supervised learning algorithm based on the Bayes theorem and used to solve classification problems. Naïve Bayes Classifier is a simple and effective Classification algorithm that builds fast machine learning models for quicker predictions. The Naïve Bayes algorithm is based on a probabilistic classifier thatpredicts based on the probability of an occurrence.

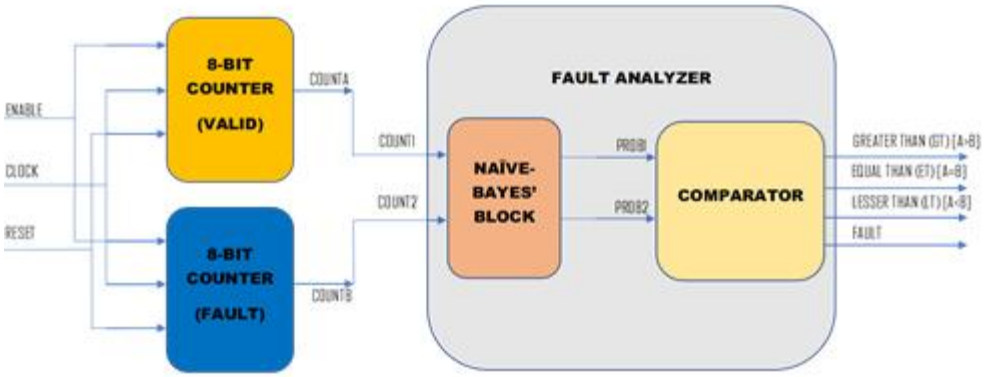

Fig. 1: Block Diagram for the proposed Fault Analyzer using Naïve Bayes method

In this work, the two 2^8-bit counters are considered and the circuit counts from "0" to "255". The Valid counter displays the output of the count from 0 to 255 for clock triggering. Similarly, the Fault counter depicts the output with a random fault instance in the counter for the clock triggering. These two counters are accumulated together to manipulate the probability of the fault occurrence and

no-fault based on the formula given below

$$P\left(\frac{A}{B}\right) = \frac{P\left(\frac{B}{A}\right)P(A)}{P(B)}$$

The naïve Bayes algorithm calculates the probabilities of the two counters from the signal inputs of "counta" and "countb". These signals "counta" and "countb" are taken into account for the Naïve Bayes Block and the evaluated counts are expressed as "count1" and "count2". These count values are allotted with evaluated probabilities each of which is the function of the Naïve-Bayes parameters and converted to the digitalized

probability equivalent. The digitalized probability equivalents of the counters are compared with the comparator circuit to give two possible outcomes of either with error or no error. The magnitude of error is evaluated using the relational comparison of the values.

To implement the proposed method in the hardware, the proposed fault analyzer is developed using the HDL code and evaluated using Xilinx. Initially, the proposed method is developed using HDL code for simulation verification by ModelSim Tool. After the simulation, the developed code is checked for synthesizabilityby making use of the Xilinx Tool. Further, the IC layout is accomplished by converting the HDL code of the proposed method using the cadence tool.

III Results and Discussions

The proposed naïve Bayes algorithm-based fault identification for the digital counter circuit is developed using the HDL code. The developed HDL code is designed using the behavioral model with the if-else block. The proposed method is developed in HDL code for simulation verification as presented in Figures 2 and 3. Figure 2 represents the counter output without errors and Figure 3 depicts the counter output with errors and indicates the occurrence of errors in the simulated output. The proposed method is real time validated by implementing in the Xilinx Tool. The RTL schematic for the proposed method using the Xilinx Tool is shown in Figure 4. Also, the area is evaluated using Xilinx Tool that uses 13% of LUTs and Occupied slices as presented in Table 1. Figure 5 gives the power report for the HDL code of the proposed methods using the Xilinx Tool. For the sake of developing the layout plan for the proposed method, the validated HDL is converted to the RTL schematic using the Genus Tool as shown in Figure 6. The IC layout can be obtained with the use of the INNOVUS cadence tool as depicted in Figure 7. The proposed method is analysed for power report using the Cadence Tool is given in Figure 8.

Fig. 2: Simulation output for the counter circuit without error using ModelSim Tool

Fig. 3: Simulation output for the proposed fault identifier using ModelSim Tool

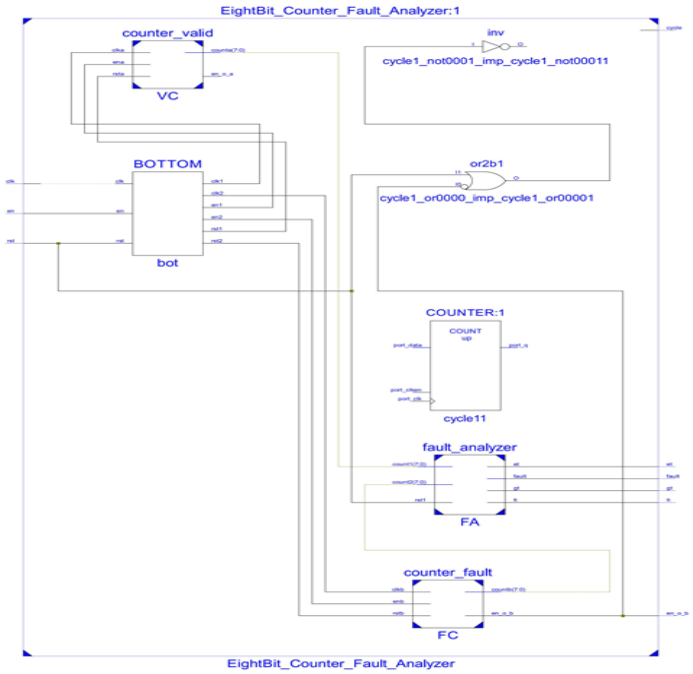

Fig. 4: RTL Schematic for the counter circuit fault identifier in Xilinx Tool

Table 1 Area Utilization chart for the counter circuit fault identifier in Xilinx Tool

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	526	9,312	5%	
Number used as Flip Flops	13			
Number used as Latches	513			
Number of 4 input LUTs	1,231	9,312	13%	
Number of occupied Slices	624	4,656	13%	
Number of Slices containing only related logic	624	624	100%	
Number of Slices containing unrelated logic	0	624	0%	
Total Number of 4 input LUTs	1,240	9,312	13%	
Number used as logic	1,231			
Number used as a route-thru	9			
Number of bonded IOBs	9	232	3%	
IOB Latches	3			
Number of BUFGMUXs	2	24	8%	
Average Fanout of Non-Clock Nets	4.55			

Device	
Family	Spartan3e
Part	xc3s500e
Package	fg320
Temp Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.2,06-23-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	4	---	---
Logic	0.000	1240	9312	13
Signals	0.000	927	---	---
IOs	0.000	9	232	4
Leakage	0.081			
Total	0.081			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	26.1	82.9	27.1

Supply Summary				
Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.026	0.000	0.026
Vccaux	2.500	0.018	0.000	0.018
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.081	0.000	0.081

Fig. 5:Power Output for the counter circuit fault identifier in Xilinx Tool

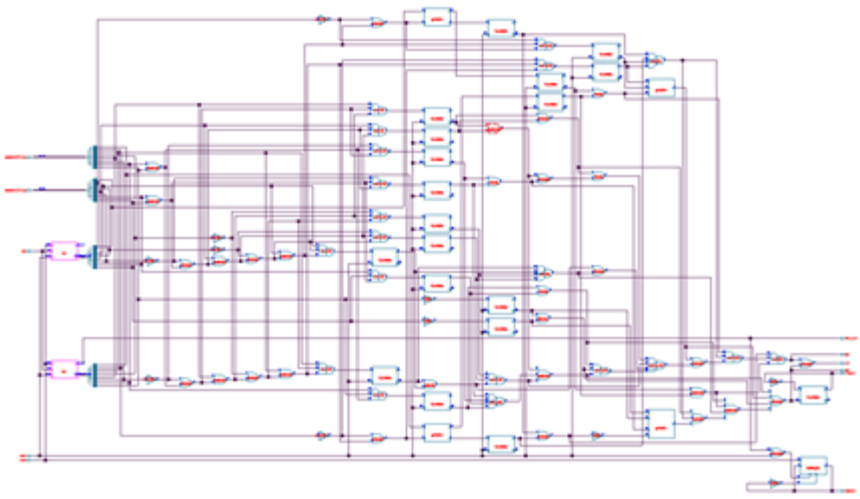

Fig.6: RTL schematic for the counter circuit fault identifier inGenus Cadence Tool

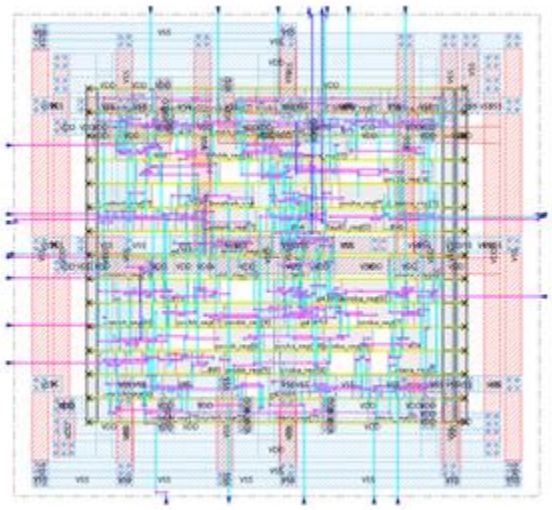

Fig.7: IC layout plan for the counter circuit fault identifier inInnovus Cadence Tool

Total Power

Total Internal Power:	0.26148932	85.3188%
Total Switching Power:	0.03658932	11.9384%
Total Leakage Power:	0.00840650	2.7429%
Total Power:	0.30648513	

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.1836	0.01259	0.003886	0.2001	65.29
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.07786	0.02399	0.00452	0.1064	34.71
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.2615	0.03659	0.008406	0.3065	100

Fig. 8:Power Report for the counter circuit fault identifier in Cadence Tool

IV Conclusion

The proposed counter circuit fault identifier is successfully designed by the inculcation of the Naïve Bayes algorithm. The real application suitability is achieved using Xilinx EDA tool with the power of 0.081W and in the Cadence tool with the power of 0.3065W. The design of layout plan for the counter circuit fault identifier is achieved by the Innovus Cadence EDA Tool.

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