Tuijin Jishu/Journal of Propulsion Technology
ISSN: 1001-4055
Vol. 44 No. 4 (2023)

# A Comparative Analysis of Low Power Schmitt Trigger Circuits in Advanced Semiconductor Technologies

**Anjana Harshitha Reddy Ganugapanta[1], Tirumala Krishna Battula[2], Prasanthi Badugu[3]**

*E.C.E.Department, University College of Engineering Kakinada, JNTUK, Kakinada, Andhra Pradesh, India*

***Abstract:*** This paper presents an extensive investigation into Schmitt trigger circuit design, with a focus on developing a Voltage Bootstrapped Schmitt Trigger (VB-ST) circuit optimized for efficiency and noise immunity. The analysis encompasses critical parameters like power consumption, leakage power, and propagation delay under various operating conditions, including different temperatures. Across semiconductor technology models spanning 90nm CMOS, BSIM4, and advanced 7nm FINFET technologies, both self-bias and non-self-bias configurations are examined. The results highlight the clear advantages of the self-biased VB-ST design, consistently outperforming its non-self-biased counterpart. It achieves lower average power consumption and leakage power while demonstrating faster propagation delays, making it an ideal choice for applications requiring rapid response times. The use of NMOS transistors for voltage bootstrapping minimizes negative bias temperature instability (NBTI) effects, enhancing its aging resilience. The incorporation of voltage bootstrapping and a feedback loop further enhances noise immunity and extends voltage swing capabilities. Consequently, the self-biased VB-ST circuit proves highly suitable for applications such as signal conditioning, noise filtering, waveform shaping, analog-to-digital conversion, and power management in electronic systems, particularly in advanced semiconductor technologies.

***Keywords****: Voltage-bootstrapping, self-bias, 90nm CMOS technology, BSIM 4 technology Model, 7nm FINFET technology model*

## 1. Introduction

This paper deals with electronic circuit design, driven by the demand for energy-efficient and high-performance integrated circuits (ICs). It underscores the role of Complementary Metal Oxide Semiconductor (CMOS) technology in overcoming the limitations of Bipolar Junction Transistor (BJT) technology, such as high power consumption, low input impedance, and limited noise immunity. CMOS technology has evolved, scaling down transistor size[1] to minimize power dissipation while maintaining circuit reliability. However, scaling introduces new challenges like reduced noise immunity, susceptibility to radiation-induced soft errors, and effects due to aging such as Negative BiasTemperature Instability (NBTI) [2].

In the realm of IC design, Schmitt triggers (STs) play a crucial role. STs, known for their wide hysteresis characteristics, effectively mitigate noisy input signals and enhances delay responses at the output.In this paper various Schmitt trigger circuit topologies are analyzed, with a primary focus on their performance in low-power applications.

The goal is to identify design techniques that minimize power consumption while preserving the reliability and functionality of Schmitt triggers. The study employs analysis, practical simulations, and measurements to evaluate different Schmitt trigger configurations for specific applications requiring low-power.These insights have broad applications including biomedical devices, smart sensors, wearable technologies, and energy harvesting systems. This paper also provides an overview of Schmitt trigger circuits, their evolution into CMOS

Schmitt Triggers [3], and existing designs with their associated limitations. It introduces the innovative concept of Voltage Bootstrapped Schmitt Trigger (VB-ST) [4] circuits, primarily utilizing NMOS transistors for feedback and voltage bootstrapping.

This paper explores VB-ST designs in the context of different semiconductor technology models, such as 90nm CMOS, BSIM4 [5], and advanced 7nm FINFET [6] technology models, emphasizing the significance of self-bias [7] and without self-bias configurations in advanced semiconductor technologies.

## 2. Objectives

The project aims to achieve the following objectives:

**Circuit Design Optimization:** The project seeks to design a Schmitt trigger circuit that is highly efficient in terms of power consumption and leakage power while maintaining fast propagation delays. This optimization includes the use of innovative techniques like voltage bootstrapping and feedback mechanisms.

**Comparison of Circuit Configurations:** The project aims to compare and analyze the performance of both self-biased and non-self-biased configurations of the VB-ST circuit. This comparison involves evaluating various critical parameters such as power consumption, leakage power, and propagation delay under different operating conditions, including temperature and voltage variations.

**Technology Analysis:** The project intends to analyze and assess the performance of the VB-ST circuit across different semiconductor technology models, including 90nm CMOS, BSIM4, and advanced 7nm FINFET technologies. This analysis helps identify the circuit's suitability and limitations across various technological platforms.

**Enhanced Noise Immunity:** The project focuses on enhancing the noise immunity of the VB-ST circuit through the incorporation of voltage bootstrapping and feedback mechanisms. This aspect is crucial for applications that require robust noise filtering and waveform shaping.

**Application Suitability:** The project evaluates the VB-ST circuit's suitability for various applications, including signal conditioning, noise filtering, waveform shaping, analog-to-digital conversion, and power management. It seeks to identify the specific use cases where this circuit design excels.

**Highlighting Self-Biasing:** The project emphasizes the importance of self-biasing in optimizing the performance of the VB-ST circuit, particularly in advanced semiconductor technologies. It demonstrates how self-biasing contributes to improved circuit performance across temperature variations.

Overall, the project aims to design, analyze, and optimize the Voltage Bootstrapped Schmitt Trigger (VB-ST) circuit for improved efficiency, noise immunity, and performance across different semiconductor technologies, with a specific focus on the advantages of self-biasing. The ultimate goal is to provide valuable insights and a well-characterized circuit design suitable for various digital signal processing and communication applications in contemporary electronic systems.

## 3. Methods

Previous logic designs have been studied to notice a ST design which is efficient.In [8] in 2003 ,the modeling of CMOS inverter was given by S.M. Kang and Y. Leblebici in their book IC’s utilizing CMOS where their main benefits include extremely low steady-state power dissipation, caused by leakage currents. The voltage swing at the output is between 0V and VDD, and the VTC transition is typically abrupt resembling that of an ideal inverter.But, it has limitations in dealing with noisy signals at the input and may exhibit sensitivity to small input fluctuations.CMOS inverter design and analysis using 90nm technology is shown in Fig .1

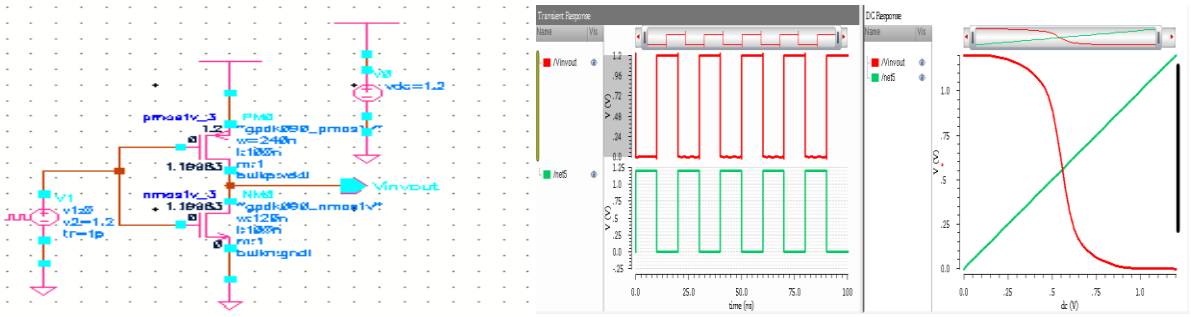

**Fig.1: Schematic, Transient and DC analysis of CMOS Inverter**

In 2016, L. A. P. Melek, etc. in their paper analyzed the classical CMOS Schmitt trigger design and it's operation in sub-threshold operation[9], but this circuit is more effected by NBTI.The move from a CMOS inverter to a CMOS Schmitt trigger was driven by the need for improved noise immunity and hysteresis characteristics. The pull-up network consisting of 3 PMOS transistorswhich enhances the aging effect, delay and decreases the reliability of the circuit. CMOS Schmitt trigger design and analysis using 90nm technology is shown in Fig.2 and it's Hysteresis is shown in Fig.3.

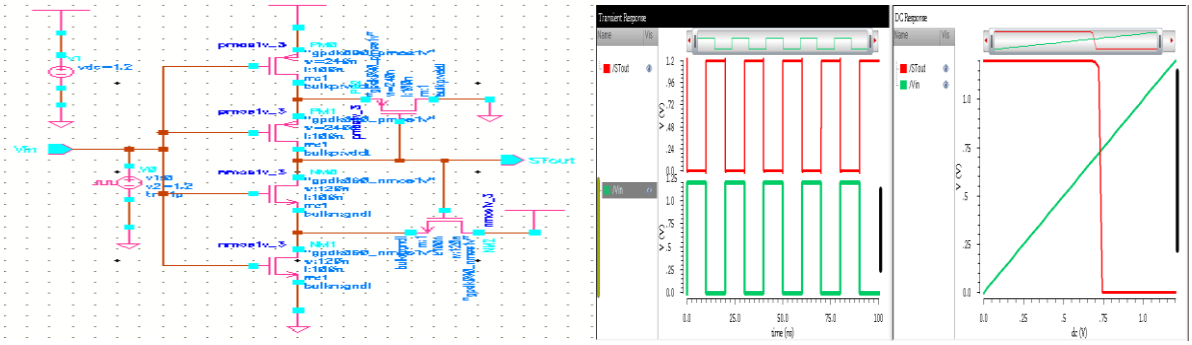

**Fig 2: Schematic, Transient and DC analysis of CMOS Schmitt Trigger**

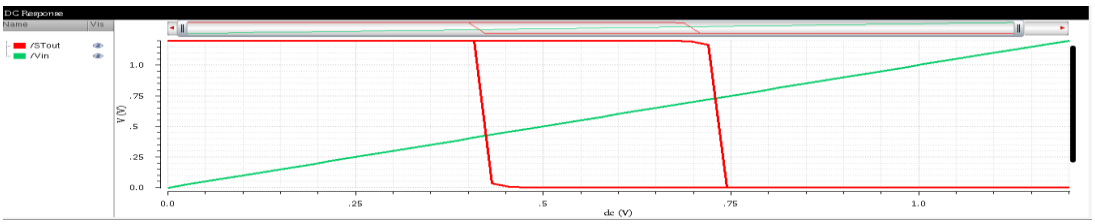

**Fig 3: Hysteresis Sweep of CMOS Schmitt Trigger**

In 2020, in their paper [10], A. P. Shah and colleagues undertook enhancement analysis of a soft error toughened and NBTI resistant Schmitt trigger (ST) circuit discovering that the NST-VB circuit has a greater potential for impact than CMOS based inverters and CMOS Schmitt Trigger .The diagram below shows analysis of NMOS alone schmitt trigger circuit including voltage booster (NST-VB) along with design. The pull-down network (PDN) is ON because of the always ON state of the pull-up network (PUN), causing direct current to flow from VDD to ground which results in a lower maximum output voltage and smaller noise tolerance for the NMOS inverter.

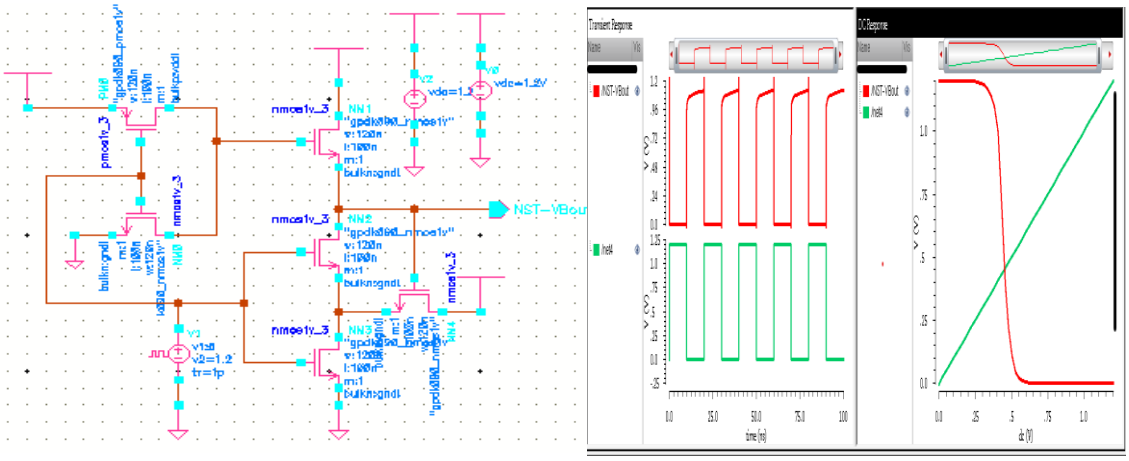

**Fig.4:Schematic , Transient and DC Analysis of NST-VB circuit**

**VB-ST Circuit with and without self-bias using 90nm CMOS technology model transistors:**

The Voltage Bootstrapped Schmitt trigger circuit without self-bias [11] and analysis is shown in the Fig.5. The previous circuit schematics and their response to square input is shown in Fig.6. The transient and DC analysis for sine input is shown in Fig.7. A circuit which is shown in Fig.8, is the voltage bootstrapped schmitt trigger circuit with self-bias and it's transient response at different temperatures is shown in the same figure and Fig.9. The arrangement of NMOS transistors in the circuit is given below:

- The NM0 transistor is used to get the output voltage swing at the output node by maintaining the threshold voltage(Vth). So, maximum voltage swing can be observed while switching.
- The transistor NM1 transfers supply voltage to output (VB-STout) .This NM1 is the pull-up transistor.
- The transistor NM2 is taken as a dummy transistor, used for the voltage bootstrapping .It acts as a MOS capacitor by connecting the source and drain terminals . This voltage bootstrapping arrangement will solve the problem of threshold voltage drop, mainly in NMOS transistor present circuits.
- NM3, NM4 and NM5 transistors are used to increase the noise immunity because they manage feedback mechanism
- All the above arrangement is for VB-ST without self-bias and for self-bias the circuit remains same except for NM5 transistor which is self-biased in the feedback.

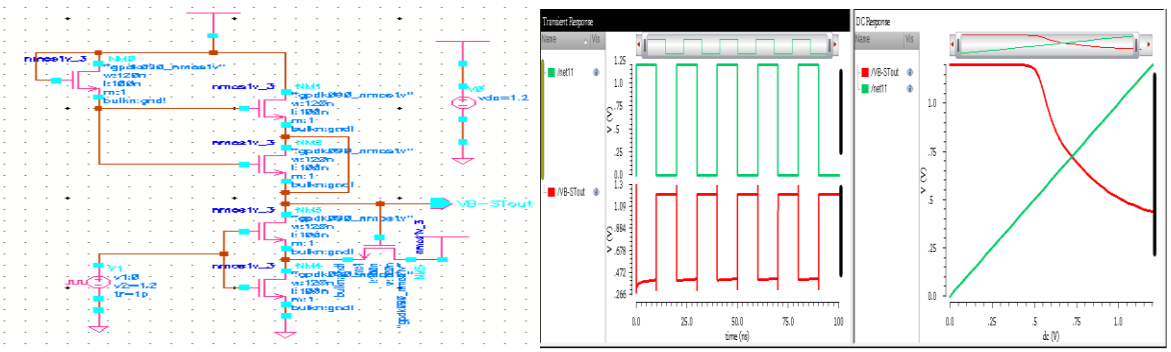

**Fig.5 Schematic and DC and Transient Analysis of (VB-ST) circuit without self-bias [11]**

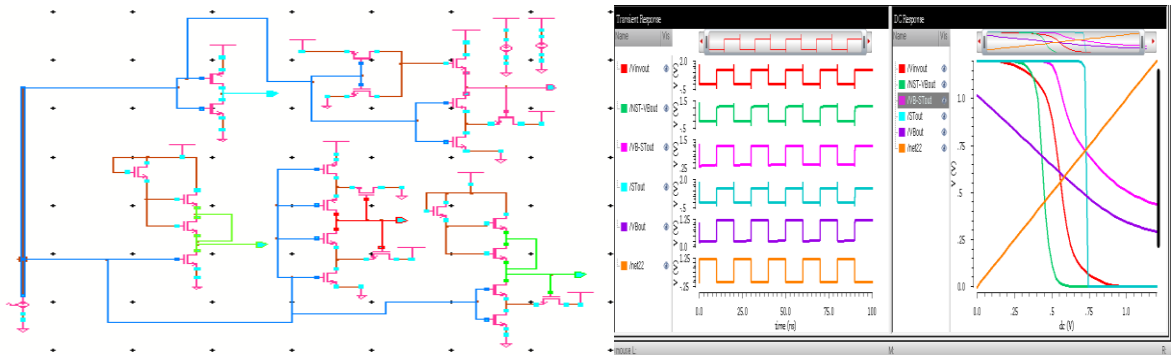

**Fig.6 Schematic ,Transient and DC Analysis of all circuits for pulse input**

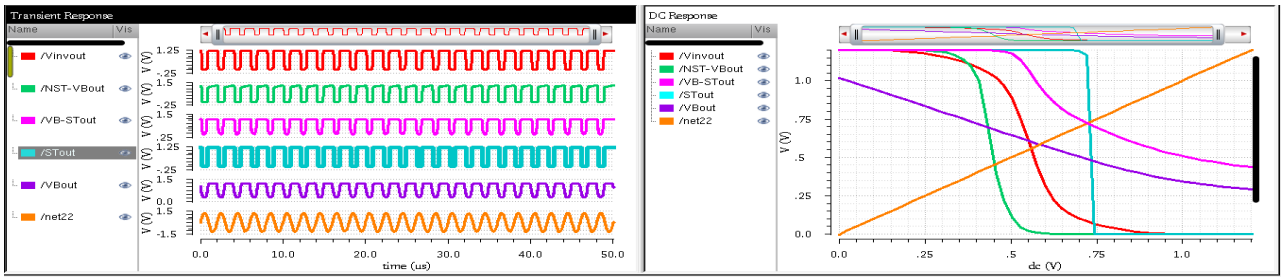


**Fig.7 Transient and DC Analysis of all circuits for sine input**

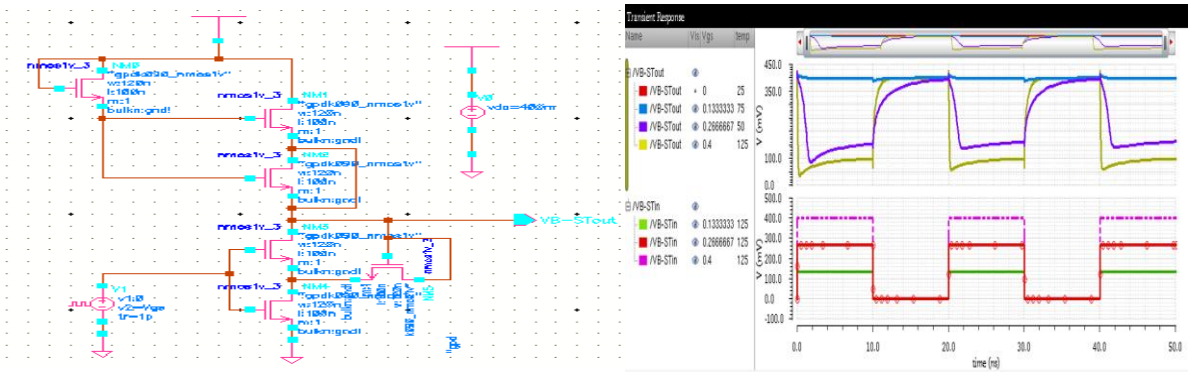


**Fig.8 Schematic of VB-ST circuit with self-bias and it's transient response**

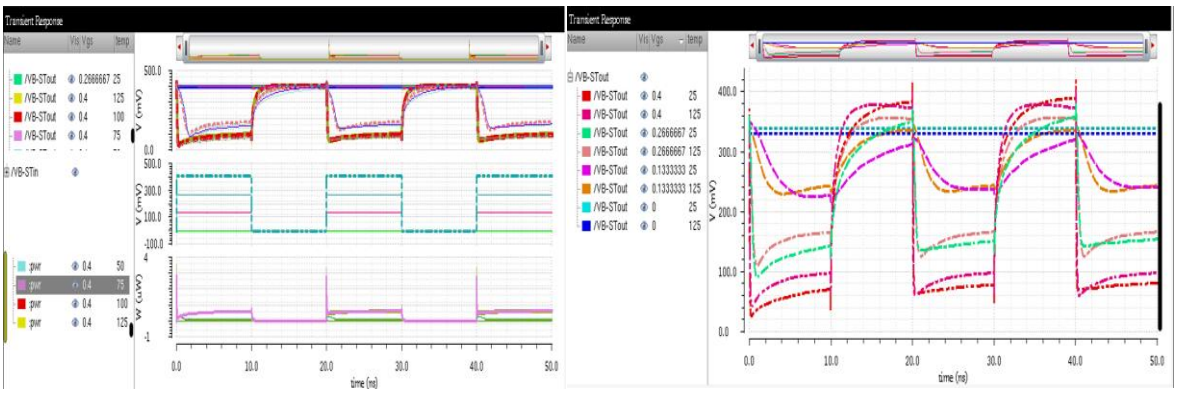


**Fig.9 90nm VB-ST without self-bias and with self-bias transient response at different temperatures and input voltages**

As a result of aging, the mobility of the carriers and the transconductance in transistors decreases, increasing the threshold voltage. Transistors must be stacked in order to combat NBTI aging effects and Hot Carrier Injection (HCI). Transistor stacking refers to the technique of arranging multiple transistors in series or parallel to achieve a desired performance or characteristics in a circuit. By arranging transistors in a series configuration, the circuit becomes less susceptible to noise and voltage fluctuations, resulting in improved reliability and robustness. The operation of an NMOS-based Voltage Bootstrapped Schmitt Trigger (VB-ST) [12] circuit is centered on the utilization of NMOS transistors in stacked arrangement.

**BSIM4 technology Model:**

The use of BSIM4 technology modelsto build and analyse the Voltage Bootstrapped Schmitt Triggers (VB-STs) is a development in semiconductor design. BSIM4 is renowned for its exceptional accuracy in modeling transistor behavior, especially in sub-micron and nanoscale technology nodes, where it captures short-channel effects, process variations, and high-frequency characteristics. Additionally, BSIM4 accounts for temperature and voltage dependencies, enabling the design of circuits capable of operating across a wide range of conditions. This industry-standard model simplifies integrated circuit design. BSIM4-based VB-STs excel in applications requiring precise modeling and optimization of transistor behavior, such as signal conditioning, noise filtering, and waveform shaping. Overall, the integration of BSIM4 technology enhances accuracy, performance, and reliability of VB-STs.

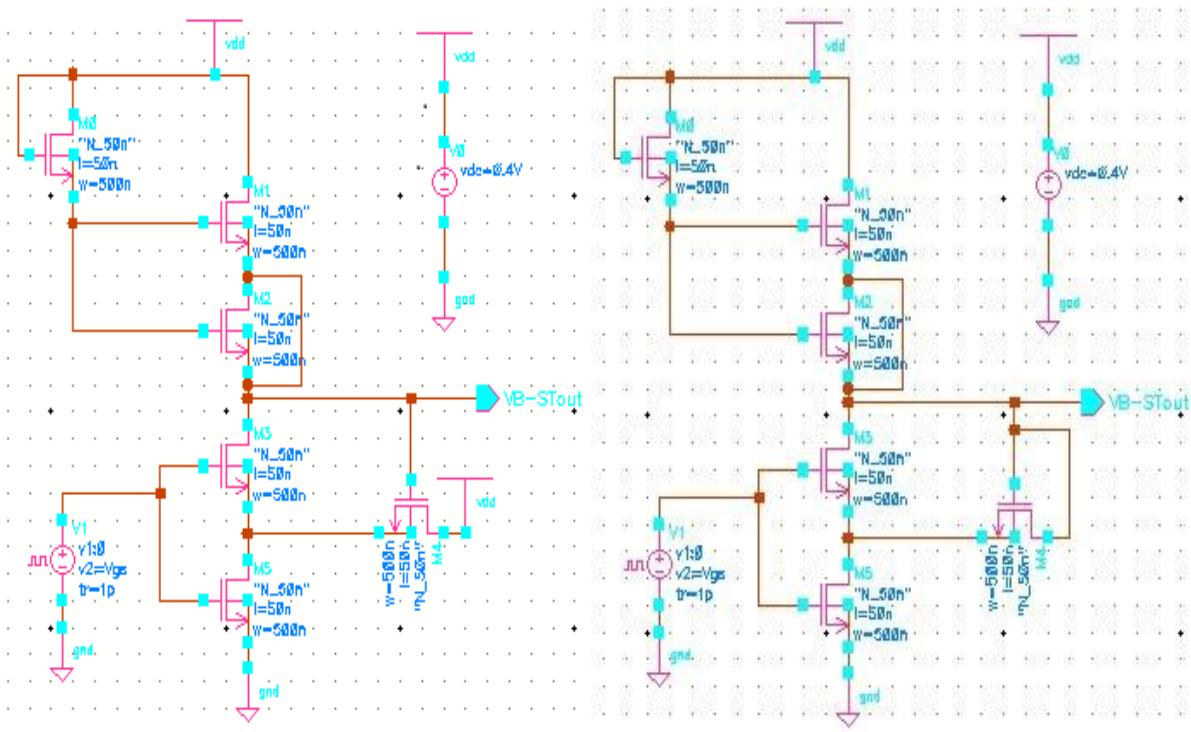


**Fig.10 BSIM4 based VB-ST circuit without and with self-bias**

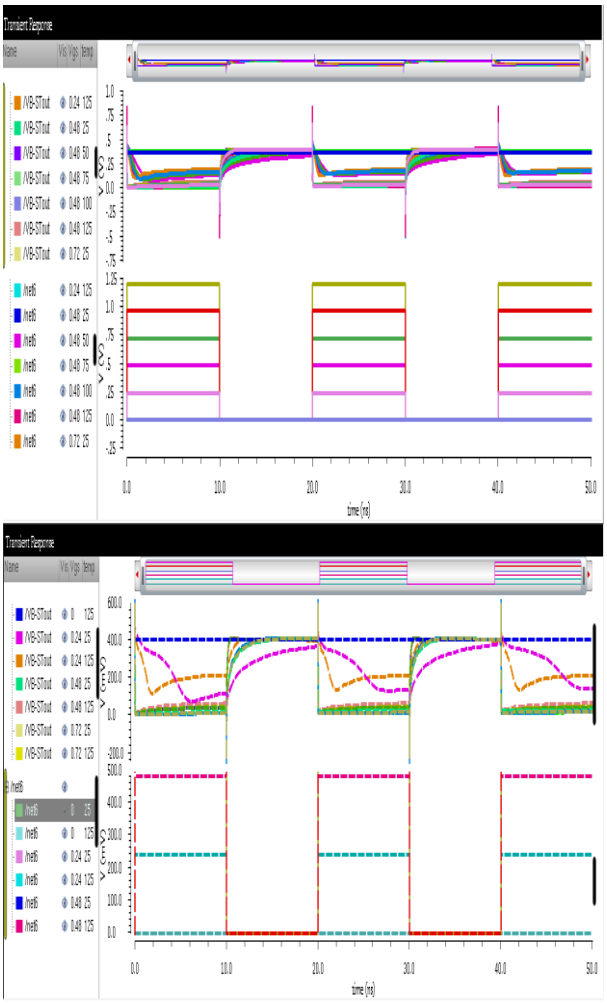

**Fig.11 BSIM4 VB-ST without self-bias and with self-bias transient response at different temperatures and input voltages**

**7nm FinFET (Fin Field-Effect Transistor) technology:**

7nm FinFET (Fin Field-Effect Transistor) technology models can be used as a replacement for traditional NMOS (N-channel Metal-Oxide-Semiconductor) and BSIM4-based NMOS transistors. Firstly, FinFETs effectively address short-channel effects (SCEs), a critical concern in advanced semiconductor technologies like 7nm, due to their three-dimensional fin structure, which offers better control over channel properties. This mitigates issues like drain-induced barrier lowering (DIBL) and threshold voltage roll-off, particularly problematic in planar NMOS transistors.Further, FinFETs exhibit lower off-state leakage current compared to their planar counterparts, a vital feature for power-sensitive applications where minimizing standby power consumption is paramount. Their scalability, manufacturing compatibility, and support from advanced transistor models like BSIM-CMG [13] further solidify FinFET technology as a preferred choice for contemporary integrated circuit designs. The use of the FinFET technology model files reduces the leakage power, average power and propagation delay of the circuits also the self-biased VB-ST shows more improvement in reduction of delay and leakage power over non self-biased VB-ST circuit.

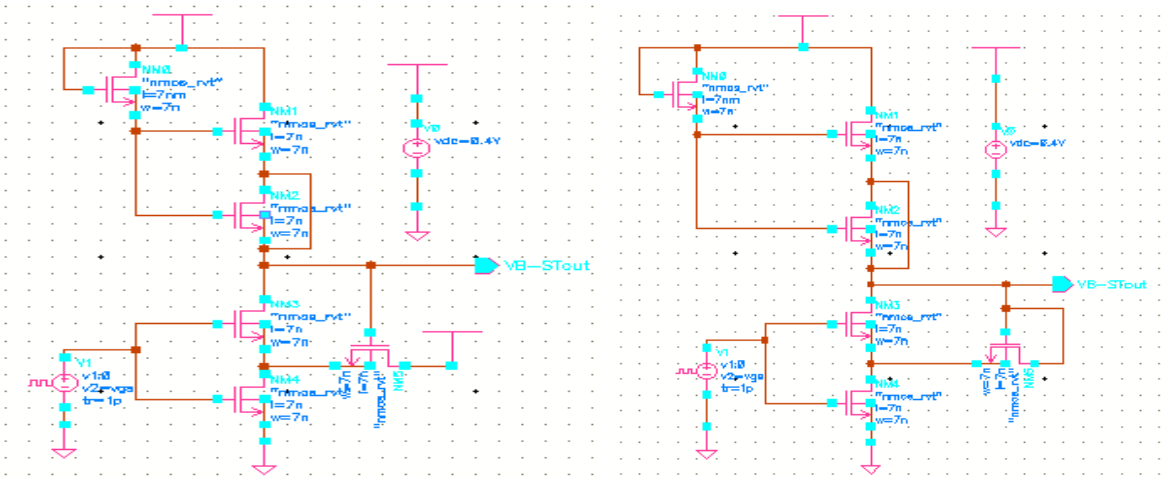


**Fig.12 7nm FINFET based VB-ST circuit without and with self-bias**

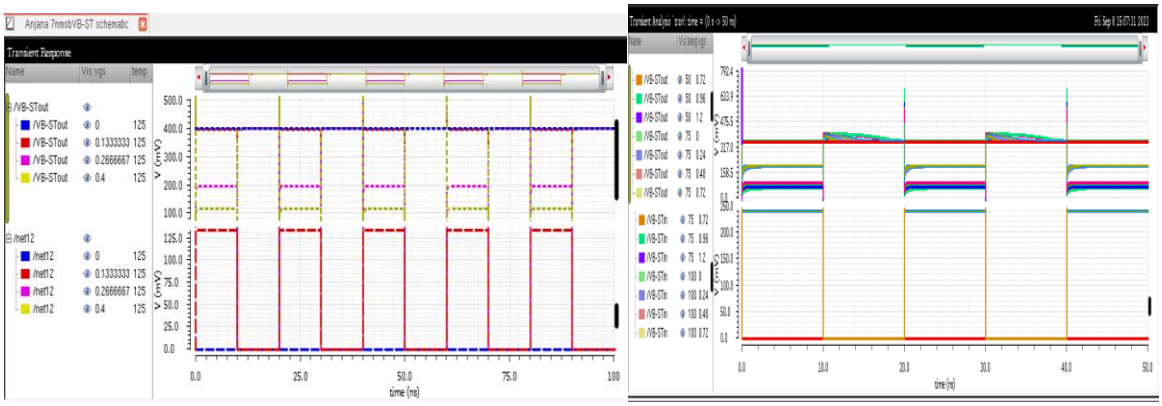


**Fig.13 7nm FINFET VB-ST without self-bias and with self-bias transient response at different temperatures and input voltages**

4. **Results :**

**Table 1: Performance Comparison of Different logic Circuits**

| Logic Design | 90nm CMOS Technology | | | |
|---|---|---|---|---|
| | LeakagePower(nW) | Average Power(uW) | Delay(ps) | Total Noise(V/sqrt(Hz)) |
| CMOS | 52.6 | 0.905 | 19.53 | 0.012m |
| ST | 32.21 | 0.331 | 25.84 | 0.521m |
| VB | 31.67 | 36.11 | 14.02 | 1.455m |
| NST-VB | 81.11 | 0.225 | 8.38 | 0.778m |
| VB-ST | 31.66 | 0.343 | 9.575 | 0.469m |

**Table 2: Comparative Analysis of Voltage Bootstrapped Schmitt Trigger Circuits in 90nm CMOS Technology at Different Temperatures**

| TEMPERATURE ($^0$C) | 90nmCMOS Technology Voltage Bootstrapped Schmitt Trigger without self-bias at 0.4V input | | | 90nmCMOS Technology Voltage Bootstrapped Schmitt Trigger with self-bias at 0.4V input | | |
|---|---|---|---|---|---|---|
| | AP (nW) | LP (nW) | D (ps) | AP (nW) | LP(nW) | D (ps) |
| 25 | 395.3 | 1.05 | 79.8 | 396.1 | 0.90 | 60.01 |
| 50 | 373.4 | 1.66 | 89.4 | 373.2 | 1.39 | 66.60 |
| 75 | 350.1 | 2.44 | 100 | 348.7 | 2.07 | 73.74 |
| 100 | 327.8 | 3.43 | 111 | 325.2 | 2.94 | 81.21 |
| 125 | 306.9 | 4.99 | 120 | 303 | 4.38 | 87.75 |

**Table 3: Comparative Analysis of VB-ST Circuits using BSIM4 Technology Models at Different Temperatures**

| TEMPERATURE ($^0$C) | BSIM4 Technology Model based VB-ST without self-bias at 0.4V input | | | BSIM4 Technology Model basedVB-ST with self-bias at 0.4V input | | |
|---|---|---|---|---|---|---|
| | AP (uW) | LP (nW) | D (ns) | AP (nW) | LP (nW) | D(ns) |
| 25 | 0.68 | 0.63 | 10 | 60.4 | 0.62 | 1.44 |
| 50 | 1.14 | 1.46 | 10 | 89.9 | 1.45 | 1.03 |
| 75 | 1.60 | 3.02 | 10 | 127 | 2.99 | 0.76 |
| 100 | 1.86 | 5.70 | 10 | 173 | 5.64 | 0.60 |
| 125 | 1.76 | 9.99 | 10 | 230 | 9.85 | 0.48 |

**Table 4 Comparative Analysis of VB-ST Circuits using 7nm FINFET Technology Models**

| TEMPERATURE ($^0$C) | 7nm FINFET Technology Model based VB-ST without self-bias at 0.4V input | | | 7nm FINFET Technology Model based VB-ST with self-bias at 0.4V input | | |
|---|---|---|---|---|---|---|
| | AP (pW) | LP (nW) | D (ps) | AP (pW) | LP(nW) | D(ps) |

| | | | | | | |
|---|---|---|---|---|---|---|
| 25 | 19.3 | 0.32 | 2.79 | 80.4 | 0.33 | 2.66 |
| 50 | 0.90 | 0.81 | 2.66 | 79.4 | 0.82 | 2.52 |
| 75 | 1.99 | 1.80 | 2.53 | 78.0 | 1.80 | 2.40 |
| 100 | 1.61 | 3.57 | 2.41 | 76.6 | 3.55 | 2.28 |
| 125 | 1.23 | 6.52 | 2.30 | 75.2 | 6.44 | 2.18 |

## 5. Discussion

From the table.1 we can observe that for low power consumption and for a combination of low average power, and low delay, VB-ST boasts a remarkably low delay, striking a balance between power efficiency and performance [15]. ST and VB designs have relatively high leakage power and may not be the best choices for designs which require power-efficiency.VB-ST demonstrates the lowest total noise level, indicating it is less susceptible to noise disturbances compared to VB and has better noise performance compared to ST and NST-VB. In conclusion, VB-ST stands out as an excellent choice for fast and noise-immune circuits within the context of 90nm CMOS technology. It offers a good balance of low power consumption, reasonable delay, and superior noise immunity compared to the other designs presented in the table.

The table.2 illustrates a compelling advantage in favor of the self-biased Voltage Bootstrapped Schmitt Trigger (VB-ST) circuit across diverse operating conditions. In comparisons between self-bias and non-self-bias configurations under different temperatures (25°C, 50°C, 75°C, 100°C, and 125°C) and at 0.4V supply voltage and in 90nm CMOS technology,the self-biased VB-ST consistently exhibits lower average power consumption (AP) and leakage power (LP), accompanied by faster propagation delays (D). This highlights the self-bias feature's pivotal role in enhancing power efficiency, reducing standby power wastage, and ensuring rapid signal response times, making the self-biased VB-ST an excellent choice for energy-efficient, high-performance applications in advanced semiconductor technologies.

The table.3 clearly demonstrates the superiority of the self-bias BSIM4-based Voltage Bootstrapped Schmitt Trigger (VB-ST) over its non-self-bias counterpart in multiple essential aspects. The self-bias configuration consistently exhibits exceptional power efficiency by consuming significantly less power in nanowatts, making it ideal for battery-powered and energy-efficient applications. Additionally, its lower leakage power enhances efficiency during idle states, contributing to extended battery life and reduced heat generation. Notably, the self-bias design's shorter propagation delay ensures faster signal switching and response times, catering to high-frequency applications. In summary, the self-bias BSIM4-based VB-ST stands out as the preferred choice, excelling in power efficiency, leakage power reduction, and speed, making it versatile for various electronic applications, including those requiring extended battery life and high-speed signal processing.

The table.4 underscores the vital role of self-bias in 7nm FINFET-based Voltage Bootstrapped Schmitt Trigger circuits[16]. With self-bias, the circuit excels in power efficiency, consuming significantly less picowatt power, exhibits lower leakage power, and features notably shorter propagation delays in femtoseconds, ensuring rapid signal response times and high-speed performance. In summary, self-bias is crucial for achieving energy-efficient and high-performance operation in 7nm FINFET technology circuits.

The study of low-power Schmitt trigger circuits has yielded insights leading to the development of the Voltage Bootstrapped Schmitt Trigger (VB-ST) circuit, distinct for its use of NMOS transistors and features like voltage bootstrapping, feedback mechanisms, and noise immunity enhancement. This innovative design minimizes susceptibility to NBTI influence, resulting in improved speed, reduced power consumption, and enhanced noise immunity, making it suitable for various digital signal processing and communication applications.

In summarizing the comparative analysis of the 90nm VB-ST, BSIM4-based VB-ST, and 7nm-based VB-ST circuits with and without self-bias, notable observations include the technology limitations of the 90nm VB-ST, the superior power efficiency and shorter delays of the BSIM4-based VB-ST, and the enhanced performance of the 7nm-based VB-ST with self-bias across temperature variations. This highlights the critical role of self-biasing in optimizing advanced semiconductor technology circuit performance.

**References:**

[1] Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, *"Scaling theory for double-gate soimosfet's,"* Electron Devices, IEEE Transactions on, vol. 40, no. 12, pp. 2326–2329, 1993.

[2] D. K. Schroder, "*Negative bias temperature instability: What do we understand*?" *Microelectronics.* Rel., vol. 47, no. 6, pp. 841–852,2007.

[3] "*CMOS Schmitt trigger—A uniquely versatile design component*," Nat. Semicond., Santa Clara, CA, USA, Tech. Rep. AN-140, Jun. 1975.

[4] N. Gupta, A. P. Shah, and S. K. Vishvakarma, "*BTI and Soft-Error Tolerant Voltage Bootstrapped Schmitt Trigger Circuit*," *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 1, pp. 153-155, 2021

[5] N. Paydavosi, S. Venugopalan, Y. S. Chauhan, J. Duarte, S. Jandhyala, A. Niknejad, and C. Hu, "*Bsim-spice models enable finfet and utbic designs*," IEEE Access, vol. 1, p. 201, 2013.

[6] Sairam, W. Zhao, and Y. Cao, "*Optimizing FinFET technology for high-speed and low-power design*," Proc. of GLSVLSI, 2007.

[7] Suresh A. "*A low power Schmitt Trigger design using SBT technique in 180nm CMOS technology"*[C]// International Conference on Advanced Communication, Control and Computing Technologies. 2014:533-53

[8] S-M. Kang and Y. Leblebici, "*CMOS Digital Integrated Circuits*". New York, NY, USA: McGraw-Hill Educ., 2003.

[9] L. A. P. Melek, A. L. da Silva, M. C. Schneider, and C. Galup-Montoro, "Analysis and design of the classical CMOS Schmitt trigger in sub-threshold operation," *IEEE Trans. Circuits Syst.* I, Reg. Papers, vol. 64, no. 4, pp. 869–878, Apr. 2016.

[10] A. Shah, N. Yadav, A. Beohar, and S. Vishvakarma, "*NMOS only Schmitt trigger circuit for NBTI resilient CMOS circuits,*" *Electronics Letters.*, vol. 54, no. 14, pp. 868–870, 2018.

[11] P. Shah, D. Rossi, V. Sharma, S. K. Vishvakarma, and M. Waltl, "*Soft error hardening enhancement analysis of NBTI tolerant Schmitt trigger circuit*," Microelectronics. Rel., vol. 107, Apr. 2020, Art. no. 113617.

[12] M.V.Dunga, C. H. Lin, Ali M. Niknejad, Chen-Ming Hu., "*BSIM-CMG: A Compact Model for Multi-Gate Transistors."* Springer US, 2008.

[13] G. Shahidi, "*Evolution of CMOS Technology at 32 nm and Beyond*," Custom Integrated Circuits Conference (CICC), 2007.

[14] Saini S, Veeramachaneni S, Kumar A M, et al. "*Schmitt trigger as an alternative to buffer insertion for delay and power reduction in VLSI interconnects"*[C]// TENCON 2009 - 2009 IEEE Region 10 Conference. IEEE, 2009:1-5.

[15] M. Alioto, "*Analysis of layout density in FinFET standard cells and impact of fin technology*," Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS), May 30 2010-June 2 2010

[16] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, "*Exploring Sub20nm FinFET Design with Predictive Technology Models*", DAC, 2012.