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Analytical Modeling of StackedAluminium Nitride Nanosheet FETs (AlNNFETs) for Cryogenic Applications

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Abstract

The present investigation proposes a new 2D analytical model for the Stacked Aluminum Nitride (AlN) Nanosheet Field Effect Transistor (AlNNFETs). For the first time, the 2D Poisson equation has been determined using the Linear Approximation Method (LAM) with appropriate boundary conditions. The precise analytical formulas for the variables drain current, transconductance, electric field, and channel potential are obtained in order to evaluate the device's performance. Regardless of the large electron fluxes into the channel brought on by the Nanosheet channel's interaction with the gate, the device functions at cryogenic temperatures. With a huge drive current capacity, it provides a significant scaling of the device. The Stacked Nanosheet's perpendicular layered structure enables it to achieve a low threshold voltage and hightransconductance. A good degree of consistency is found when comparing the findings of analytical models and TCAD simulation software.

Keywords: Aluminium Nitride Nanosheet (AlNNFET),Poisson Equation, Linear Approximation Method (LAM),Drain current,Transconductance, Electric Field.

1. Introduction

For analogue and digital circuits, semiconductor devices are exceedingly trustworthy and offer great promise. The present trend focuses on building low scaling devices that are more power efficient in order to meet the demands of increasingly compact and energy-efficient electronic systems. CMOS technology generations to maintain a high degree of electrostatic regulation [1–3]. Additionally, as technology develops, MOSFETs have challenges such as increased power consumption and leakage currents, which limit their usefulness in incredibly small semiconductor devices. Among the disadvantages of MOSFETs is their susceptibility to hot carrier injection, a phenomenon where high-energy carriers erode the gate oxide and may compromise the transistor's long-term reliability and performance [4-6]. Leakage voltage and leakage current are the two main causes of leakage power in switching devices.

Due to their low leakage current, FinFET devices utilize less power than MOSFETs. However, due to its 3-D profile, quantized device-width, and challenging-to-control dynamic Vth, FinFET also had very high capacitances, corner effect, and larger parasitics. FinFET costs can increase by 2-3% compared to bulk, according to manufacturing technique [7-8]. Because the gate only covers three sides of the rectangular Fin, the bottom side of the Fin touches the substrate, which is another disadvantage of FinFET technology. This causes a sizable leakage current in the transistor even when it is off-state [9–11].

Compared to FinFETs and MOSFETs, Stacked Nanosheet Field Effect Transistors (AlNNFETs) at 3 nm provide better electrostatics and short channel management. In order to provide a greater drive current than FinFETs, nanosheet transistors narrow their channels [12]. The suggested device's n-type perpendicular stacking design improves channel control and lessens short-channel effects. When Nanosheets are stacked perpendicular to each other, the effective channel width rises [13–15]. This allows Nanosheets to provide a larger driving current per channel than Fins. By putting oxide between the substrate and source/drain and stacking more Nanosheets (creating more channels), the device driving current can be raised [16, [17]. Perpendicularly stacked Nanosheet designs, which offer short channel management and good electrostatics, satisfy the requirements of logic devices at 3-nm nodes [18], [19]. A C-shaped arrangement of nanosheets perpendicular to each other can reach an equivalent channel width, which is more than four times more area-efficient than a MOSFET. This design enhances the transistor's performance by providing more control over the current flow. The vertical architecture allows for a higher integration density on a chip, which helps create more powerful and compact electronicdevices [20].

2. Device Structures and Simulations

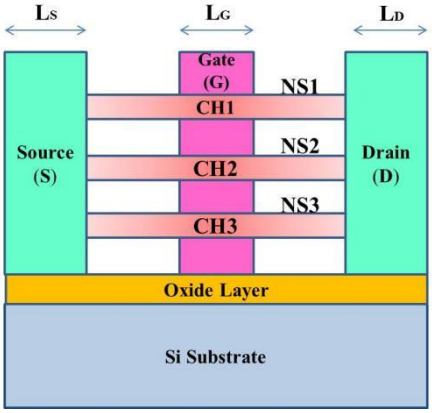

Fig. 1 Cross sectional view of AlNNFETs

With a 5.2eV work function, the gate is made of gold metal, and the stacked nanosheet is made of aluminum nitride (AlN). A two-stacked nanosheet is used to create a four-channel device with the structure of FETs. Electrons in the channel can move freely and without colliding thanks to the impact of the four channels with double nanosheet. The feasibility of the suggested device for low-power applications is clearly established by the analysis. A thin layer of Hafnium oxide material placed to both sides of a nanosheet structure is referred to as the oxide layer in double nanosheets. In order to facilitate effective electronic device operation at nanoscale dimensions, it acts as a dielectric layer, offering insulation between the nanosheets.

As seen in Fig. 1, the transistor's stacked nanosheets are positioned on the gate that is encircled by the source and drain. These Nanosheets are affixed to an AlN substrate with a thin oxide layer, and the gate is positioned vertically across them.Nanosheet transistors generate high driving current by enclosing the conduction channel with a metal gate. Stacked AlNNFETs encircle the channel to improve transistor switch control, as opposed to the FinFET architecture's three-sided approach. A greater degree of integration and functionality is attained in this work by integrating three channels into a three Nanosheet FET device. The fully stacked nanosheets have a channel structure and are heavily doped. The tiny channel region of nanosheet transistors enables the gate to provide fine control over the flow of electrons.

3. Analytical Modeling

The 2D Poisson equation is utilized to determine the electrical characteristics of the semiconductor device, with the distribution of charges and doping profiles within the AlNNFETs device [21].

$$L''_{xi}(x,y) + L''_{yi}(x,y) = \frac{-qN_d}{\varepsilon_a}, 0 \le x \le L_i, 0 \le y \le d_{eqv}, i=1, 2 \quad (1)$$

whereN_d - doping concentration, q - charge of electron,$L(x,y)$- electric potential and ε_a - permittivity of Aluminium Nitride (AlN), L - Length of the Nanosheet, d_{eqv} -total thickness of Nanosheet [22].

$$d_{eqv} = n_s(2W_{ns} + 2T_{ns}) \quad (2)$$

wheren_s is the number of Nanosheets, W_{ns} is the channel width and $T_{ns}$is the Nanosheet thickness

A perfect linear function can accurately represent the potential expression in both directions in this analysis.

$$L_i(x,y) = V_i(x,y) + V'_{xi}(x - L_i) + V'_{yi}(y - d), i=1, 2 \quad (3)$$

where$V(x,y)$ is channel potential.

3.1 Boundary conditions:

(i) At x_i=0 and y_i=0, the channel potential is at the contact of different metals.

$$L_i(x,y)|_{\substack{x_i=0\\y_i=0}} = V_g, i=1, 2 \quad (4)$$

where $V_g = V_{gs} - V_{fb}$, V_{gs} - gate-source voltage, V_{fb} - flat-band voltage

(ii) At x_i=0 and y_i=d, the electric field at the contact of different metals.

$$L'_{yi}(x,y)|_{\substack{x_i=0\\y_i=d}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}(Q_s + C_{ox}(V_{gate} - V(x,y)), i=1, 2 \quad (5)$$

(iii) Potential at x_i=0 and y_i=0 on the source end,

$$L_i(x,y)|_{\substack{x_i=0\\y_i=0}} = V_{bi}, i=1, 2 \quad (6)$$

whereV_{bi} is built-in-voltage.

(iv) Potential at x_i=L_i and y_i=0 on the drain end,

$$L_i(x,y)|_{\substack{x_i=L_i\\y_i=0}} = V_{bi} + V_{ds}, i=1, 2 \quad (7)$$

whereV_{ds} is drain-source voltage.

3.2 Channel potential model:

The potential difference that might exist at the interface generates the AlNNFETs channel potential, which could affect the device's functionality. The channel potential in AlNNFETs is significantly influenced by the gate voltage and dual channel contact. The potential at the Aluminum Nitride (AlN) channel region is calculated using the Linear Approximation Method (LAM). To produce a linear range of performance, the device's channel—which is totally depleted in the off-state—is evenly doped with a high doping concentration. Along the x and y-axes, the channel potential values are chosen at two different positions, such as $x = 0$, $x = L_i$, and $y = 0$, $y = d$.

Apply boundary conditions (4) and (5) in (3),

$$L(x,y) = V(x,y) + \frac{\varepsilon_{ox}}{2L\varepsilon_{si}t_{ox}}\left((Q_s + Q_{gate})d - \frac{V_g}{L}\right)(x - L) - \frac{\varepsilon_{ox}}{2\varepsilon_{si}t_{ox}}(Q_s + Q_{gate}) \quad (8)$$

where$Q_{gate} = C_{ox}(V_{gate} - V(x,y))$

Apply boundary conditions (6) and (7) in (1),

$$L(x,y) = -\frac{qN_d}{4\varepsilon_a}(x^2 + y^2) + \left(\frac{V_{ds}}{L} + \frac{qN_d}{4\varepsilon_a}L\right)(x + y) + V_{bi} \quad (9)$$

The total channel potential is determined by equating (8) and (9),

$$V(x,y) = \frac{k_1+k_2+V_{bi}-k_3\left(Q_s\left(\frac{x}{L}-d-1\right)+C_{ox}V_g\left(\frac{d}{L}+d-1\right)\right)}{1-k_3\left(\frac{x_d}{L}+C_{ox}(d-1)\right)} \quad (10)$$

where $k_1 = -\frac{qN_d}{4\varepsilon_a}(x^2+y^2), k_2 = \left(\frac{V_{ds}}{L}+\frac{qN_d}{4\varepsilon_a}L\right)(x+y), k_3 = \frac{\varepsilon_{ox}}{2\varepsilon_{si}t_{ox}}$

The electrons in theNanosheet are contained by the channel potential, which also enables high-frequency, high-speed operation and great electron mobility.

3.3 Electric field model:

The doping concentration of the Nanosheet channel and the gate voltage of the AlNNFETs affect the electric field's strength. High conductivity in the channel and effective electron transport are made possible by the concentration of electrons at the contact. The analytical model of the electric field has been created by differentiating the channel potential along the channel length can be found and as a result, the resulting electric fields is determined using

$E_i(x) = V'_{xi}(x,y)|_{yi=0}$, i=1, 2

The total electric field is given by,

$$E(x) = \frac{((k_4\left(-2k_5x+\frac{V_{ds}}{L}+k_5L+V_{bi}-\frac{k_3Q_s}{L}\right))(-k_5x^2+\left(\frac{V_{ds}}{L}+k_5L\right)x+V_{bi}-k_3k_6)(-k_3\frac{d}{L}))}{k_4^2} \quad (11)$$

where$k_4 = 1-k_3(\frac{x_d}{L}+C_{ox}(d-1))$, $k_5 = \frac{qN_d}{4\varepsilon_a}$, $k_6 = Q_s\left(\frac{x}{L}-d-1\right)+C_{ox}V_g\left(\frac{d}{L}+d-1\right)$

It is imperative to optimize the distribution of the electric field in order to prevent problems like breakdown voltage restrictions and hot carrier effects. The Nanosheet channel's electron density and potential are modulated by the electric field produced by the dual gate contact.

3.4 Drain current model:

The device affected by the gate voltage at the channel, which also affects the channel potential and electric field. High-mobility electrons inhabit the Nanosheetchannel, and electron transport in this channel is intimately correlated with the drain-source current. The drain current of an NSFET in the linear zone has been simplified. The following formula can be used to approximate the drain-source current in an NSFET:

$$I_{ds} = KTW\mu_0 n_i^2\sqrt{\frac{\varepsilon_{si}V_{min}(x,y)}{2N_d^2}}\left(e^{\frac{qV_{min}(x,y)}{KT}}-e^{\frac{q(V_{min}(x,y)-V_{ds})}{KT}}\right) \quad (12)$$

where$V_{min}(x,y)$ - minimum potential in channel, μ_0 – electron mobility, n_s - sheet carrier density.

3.5Transconductance:

One essential metric for describing a transistor's behavior and amplification capacity is its transconductance. A few of the variables that affect it are the channel density, carrier mobility, channel width, length and gate voltage. Greater gate length and lower noise amplification capacity are indicated by greater transconductance values. The standard notation for conductance is g_m, which can be analytically represented as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (13)$$

where∂I_{ds} - change in drain-source current, ∂V_{gs} - change in gate-source voltage

Substitute the I_{ds} value in (14), the transconductance is found by

$$g_m = \frac{KTW\mu_0 n_i^2}{N_d}\sqrt{\frac{\varepsilon_{si}}{2}}\left(\sqrt{V_{min}(x,y)} + (\alpha_2+\alpha_3)\left(\frac{1}{2\sqrt{V_{min}(x,y)}}\alpha_1\right)\right) \quad (14)$$

where $\alpha_1 = \frac{k_3^2 d}{L^2}C_{ox}(d + L(d-1))$, $\alpha_2 = e^{\frac{qV_{min}(x,y)}{KT}}$, $\alpha_3 = e^{\frac{q(V_{min}(x,y)-V_{ds})}{KT}}$

3.6 Integrated Noise:

With varying materials and gates, numerous models have anticipated noise in different parts or at the device's output. The total noise analysis's accuracy is still being improved, though. For high-frequency applications, the suggested model uses an integration technique to guarantee precise estimation of the device's total noise. Integration creates a single system that operates as total integrated noise by combining smaller noise components. This method is used to identify the noise at the output and attempts to make noise prediction easier for the entire device.

$$\overline{I_{nd}^2} = 8kT\Delta f\,\frac{g_m}{0.666\,C_0}(L_1 + L_2 + L_3)(\alpha W + \beta I_{ds}) \quad (15)$$

where$k$-Boltzmann constant, T-room temperature, Δf-bandwidth, α and $\beta$are fitting parameters whose values are $2 \times 10^5 pF/cm^2$ and $1.25 \times 10^2 pF/mA/cm$.

4. Result and Discussion

Table 1: Parameter values for AlNNFETs

Parameters	Specifications
Gate Work Function (Au)	5.1eV
Length of source & drain (L_s&L_d)	12nm
Length of gate (L_g)	16nm
Doping level of Source (N_A)	10^{20} cm^{-3}
Doping level of Drain (N_D)	10^{20} cm^{-3}
Channel Length (L)	20 nm
Oxide Thickness (t_{ox})	2nm

The Linear Approximation Method (LAM) is used to compute and validate the parameters analytically in order to study the device performance of AlNNFETs. The results of the analytical modeling and the TCAD simulator are precisely in sync. By examining the Gaussian profile with potential at the points $x = 0$and $x = L$, the parameters are retrieved. The value for parameters for AlNNFETs is shown in Table 1.

In Fig. 2, gate control and short-channel effects are balanced by a reasonable oxide thickness. The gate's effect on the channel potential is less pronounced in thicker oxides. Variations in V_{gs}cause the channel potential to react more gradually.A stronger and more focused impact on the channel potential is the outcome of improved gate control. Strong electrostatic channel control by the gate is made possible by an incredibly thin oxide. Variations in V_{gs}cause the channel potential to react more quickly and sensitively.

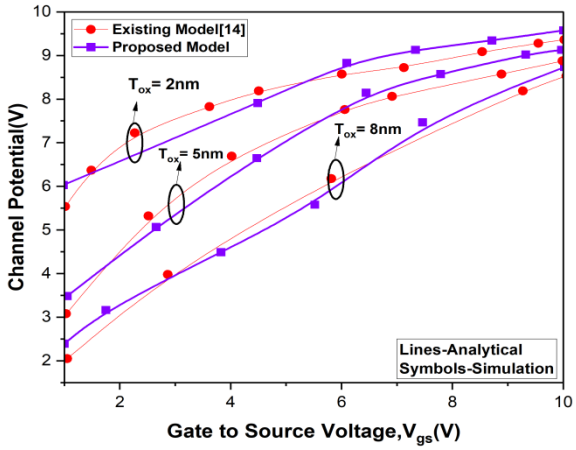

Fig. 2 Channel potential vsV_{gs} for different T_{ox}

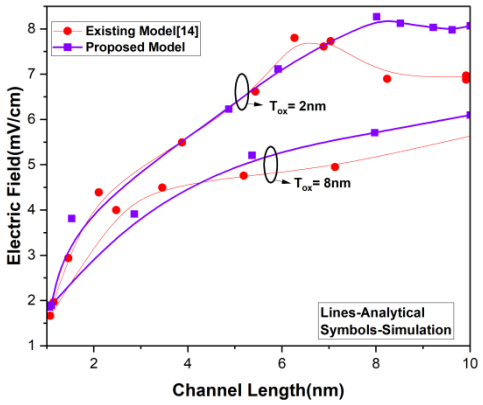

Fig. 3 Electric field versus L for different T_{ox}

In Fig. 3, an electric field peak guarantees a superior average electric field over the channel for T_{ox}=2 nm. Consequently, carrier transport efficiency and device speed both increase at T_{ox}=2 nm. The electric field is directly affected by the channel length, oxide thickness, and applied voltage. This leads to thinner oxide layers, which strengthen the observed electric field more than the existing model. The electric field is dispersed farther with an oxide thickness of T_{ox}=8nm.A less concentrated electric field could result in a more consistent behavior along the channel. A compromise between short-channel effects and gate control can be achieved with an oxide thickness of T_{ox}=2nm.Strong electrostatic channel control by the gate is made possible by the oxide thickness T_{ox}=2nm.The proposed model shows high electric field when compared to existing model.

In Fig. 4, more channel control and more effective transistor modulation are made possible by higher gate voltages, which frequently cause the drain current to increase. As V_{ds} increases, the transistor may approach the saturation area, which is the point at which the drain current reaches a maximum and subsequently starts to saturate. According to the proposed model, I_{ds} rises enables better channel control. Because of the greater carrier injection in the channel, higher V_{gs}levels often translate into higher drain current levels over the whole V_{DS} range. The proposed dual Nanosheet with quad channel shows high drain current.

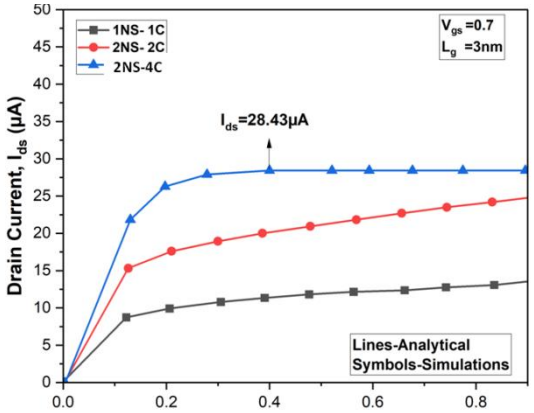

Fig. 4I_{ds}vsV_{ds} for different V_{gs}=0.7V and L_g=3nm

Because of improved electrostatic control, the transistor may encounter more short-channel effects as the channel length reduces, which would lower threshold voltage.

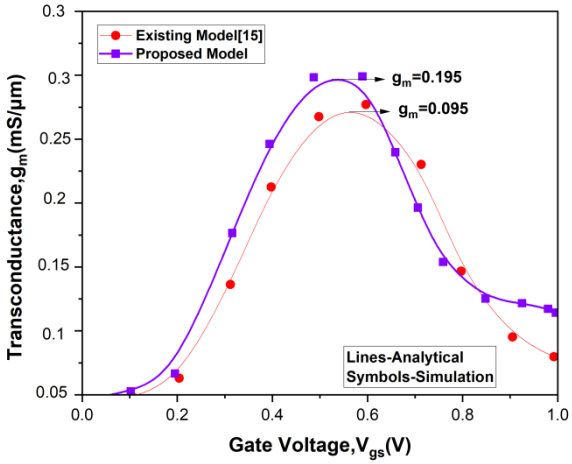

Fig. 5Transconductance versus gate to source voltage

For varying oxide thickness, the transconductance (g_m) varies with gate-source voltage is shown in Fig. 5. The conductance decreases in the saturation region due to deteriorating mobility. The electric field in the channel is stronger in the presence of peak transconductance. The gate capacitance rises as the oxide thickness decreases T_{ox}=2nm.For a change in V_{gs}, enhanced gate control causes a more noticeable change in the channel current. There may exist a threshold at very thin oxide thicknesses T_{ox}=2nm where short-channel effects become noticeable. These short-channel effects may result in a saturation or reduction in the transconductance curve at increasing V_{gs}. With improved channel control over the current model, g_m improves along with V_{gs}. In comparison to the existing model, a peak transconductance of g_m=0.195ms/μm is achieved in proposed model.

5. Conclusion

The LAM is used to generate the 2D Poisson equation and develop an analytical model for stacked nanosheet FETs. The perpendicularly stacked nanosheet FETs with better gate control than earlier devices imply high electron mobility. Short channel effects are thereby lessened. The result also shows that a drop in oxide thickness affects the device's peak electric field. The device is an excellent choice for 6G real-time applications since it has been found that the Stacked Nanosheet FETs gate significantly boosts the anticipated transconductance with g_m=0.195ms/μm. This study demonstrates that high transconductancenanosheet FET devices have a low threshold voltage (V_T=3.37V) and fast speed performance with little error. Analytical modeling and TCAD simulation results are in good agreement.

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