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ASIC Flash Analog to Digital Convertor Using Operational Amplifier

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Abstract—

Because digital signals are easier to store and send than analogue signals, they are also more dependable, secure, and accurate. Additionally, noise has less of an impact on digital transmissions than it does on analogue ones. Digital signals find widespread use in numerous applications. Signals from analogue sources are converted to digital ones using analogue to digital converters. This project aims to construct a Flash ADC with 8 bits. An EDA tool called Cadence is used to implement Flash ADC. Results of synthesis are produced for power and speed. The Flash ADC findings have been examined and contrasted.

Keywords*—Flash ADC, Analog to digital convertor,Priority encoder.*

Introduction

In the modern world, digital communication is essential since digital communications utilise less bandwidth than analogue signals and are less susceptible to noise. Analogue to Digital Converter (ADC) can be used to accomplish the analogue to digital conversion. An electrical integrated circuit that transforms an analogue voltage input into a digital number is called an analogue to digital converter.

There have been several ADC proposals made in the past. Below are some examples of earlier ADC design-related work. Increasing speed, sample rate, and resolution has been the main emphasis of research on analog-to-digital converters (ADCs) for the last ten years. Four-way interleaved very fast ADC for communication in the unlicensed frequency band about 60GHz has been published [1] together with the study and implementation of comparator in CMOS 50nm technology. Remaining gain error, DAC error, and op amp nonlinearity can be eliminated with a pipelined ADC calibration technique and a precise resistor ladder topology [2]. With a power consumption of 55 mW, the ADC reaches 53 dB SNDR claimed because to its high-speed, low-power op amp design.

A brief overview of the analogue to digital conversion process is provided in Energy-Efficient Analogue to Digital Converter for Digital Signal Processing and Classification Applications by [3]. Two steps are used to accomplish this: quantization and sampling. Certain parameters—such as resolution, SNR, and SFDR—are more crucial throughout the conversion process and are covered in this work. The ADC's performance is evaluated using quantization error, DNL, and INL, all of which have set values. ADCs come in a variety of forms, which are also discussed in the literature on this analogue to digital conversion.

Eight-bit low-power analog to digital converter (ADC) in 180 nanometers. Analog-to-Digital Converters (ADCs) are helpful building blocks in many applications, including data storage, read channels, and optical receivers in digital communication, according to CMOS Technology by [4]. This is because ADCs serve as the interface between digital signal processors and analogue signals found in the real world. Double edge triggered D-flip flops (DETDFF), which combine excellent accuracy and low power consumption, can be utilised to create ADCs with low optimum delay using standard CMOS technology and low-cost VLSI implementation. Scaled CMOS technology-based ADCs can be utilised in implantable or portable biomedical applications, as well as wireless ones, and they run on a small amount of battery power.

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I. PROPOSED METHOD

Flash ADCs use a network of comparators and a parallel comparison technique to provide quick digital conversion of analogue signals. They are appropriate for applications needing accurate and timely analog-to-digital conversion because of their speed. Block diagram of Flash ADC is shown in Fig. 1.

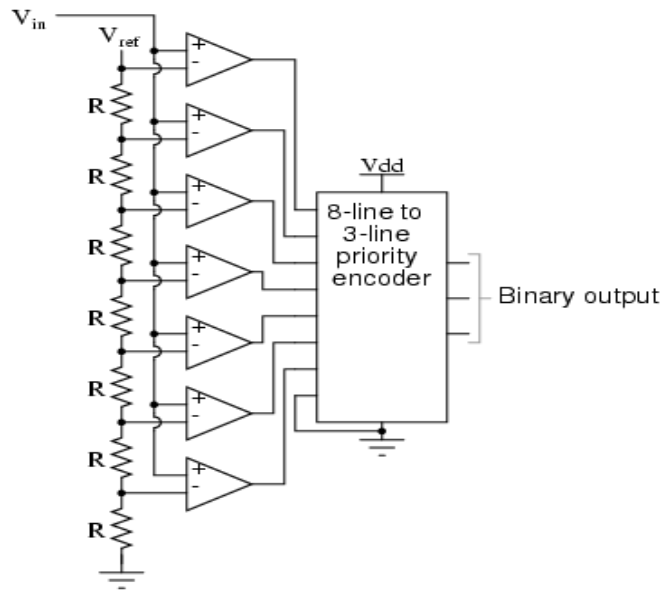

Fig.1 Block diagram of Flash ADC.

Flash ADCs transform an analogue input voltage into a digital output by means of a network of comparators.

Through the use of a ladder network of resistors, the analogue input voltage is separated into multiple voltage ranges.

In the network, each voltage range is associated with a certain comparator. The comparator network, which consists of a set of comparators equal to the number of digital bits in the output, is the brains behind a Flash ADC.

The resistor ladder network's reference voltages and the input voltage are simultaneously compared by the comparators. Every comparator produces a binary result that indicates if the input voltage is higher or lower than the reference voltage.

For the purpose of creating the digital representation of the analogue input, the binary outputs from each comparator are then concatenated. Because each comparator runs separately and in parallel, flash ADCs are renowned for their fast operation.

The number of comparators in the network determines the resolution of a Flash ADC; more comparators are needed for higher resolution. Applications including data acquisition systems, medical imaging, and telecommunications where high-speed and high-resolution conversions are essential frequently use flash ADCs. While flash ADCs are great for high-speed applications, they cannot be as power-efficient as other ADC types, particularly when resolution goes up. Based on the particular requirements of the application, designers frequently have to carefully examine trade-offs between speed, power consumption, and resolution. Operational amplifier is designed using virtuoso tool and block diagram of opamp is shown in figure2. The comparator is designed using Op-amp.

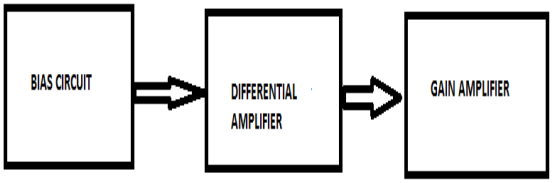

Fig.2. Block diagram of op-amp

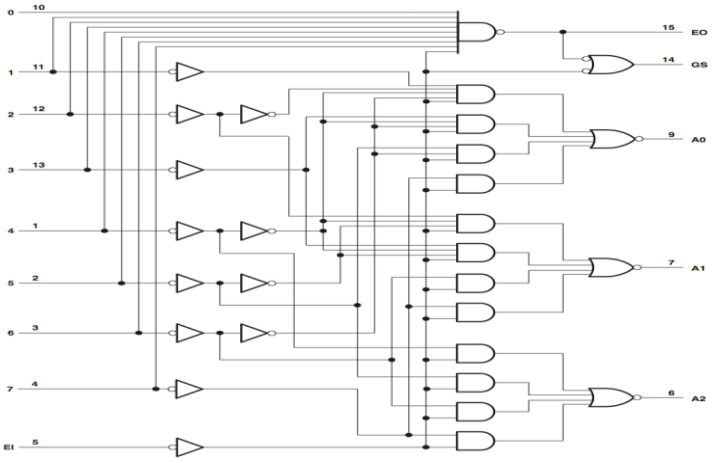

Fig3.Logic Diagram of Priority Encoder:

Figure3 shows the logic diagram of priority encoder and it is designed using cadence tool. The flash ADC is designed using comparator and priority encoder. Thus the proposed ADC has better performance than existing methods.

II. RESULTS AND DISCUSSION

The proposed method are designed as first operational amplifier is designed as per figure2 and secondly non Inverting comparator using designed op-amp and third step is design of priority encoder. These three designed blocks are used to design a flash ADC. A cadence virtuoso tool is used designing all methods. The simulation and synthesized reports are given below. The schematic of Opamp is shown in the Figure 4. Schematic diagram of Comparator using Opamp is shown in figure5. Figure 6 shows the output results of comparator. Compresses multiple no of inputs and Produces less no of outputs. The schematic diagram of an 8 to 3 priority encoder is shown in the Figure7. Flash ADC is implemented by combining the resistive network, comparator and priority encoder as shown in figure9.The flash ADC output for the analog input 7 is shown in figure10.

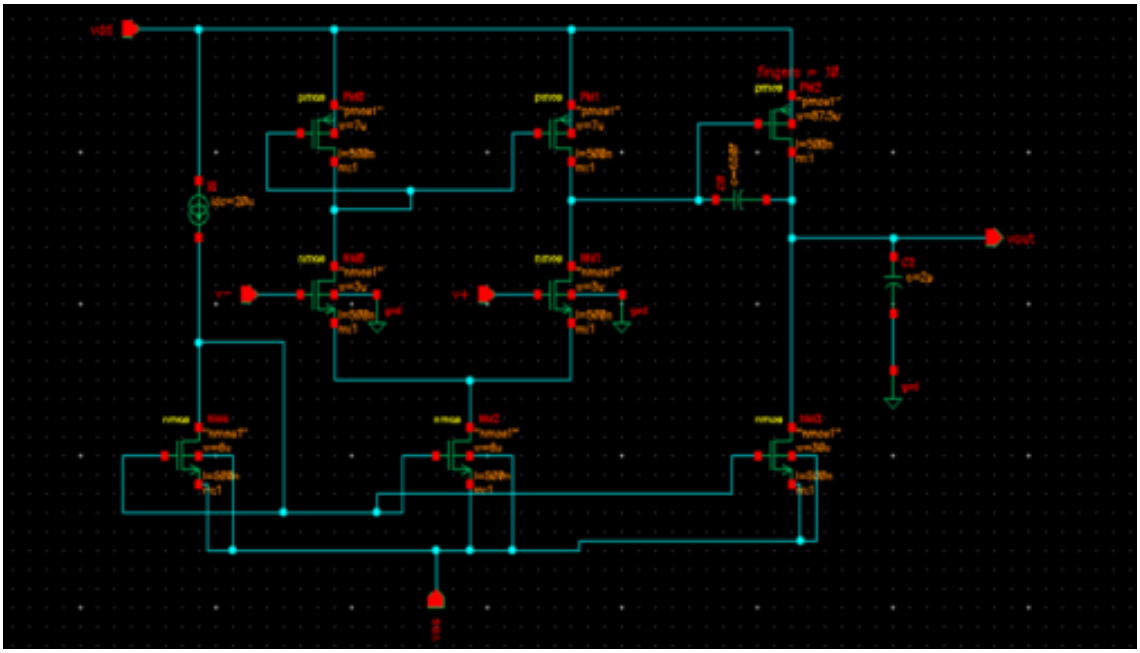

Fig.4 Schematic diagram of operational amplifier

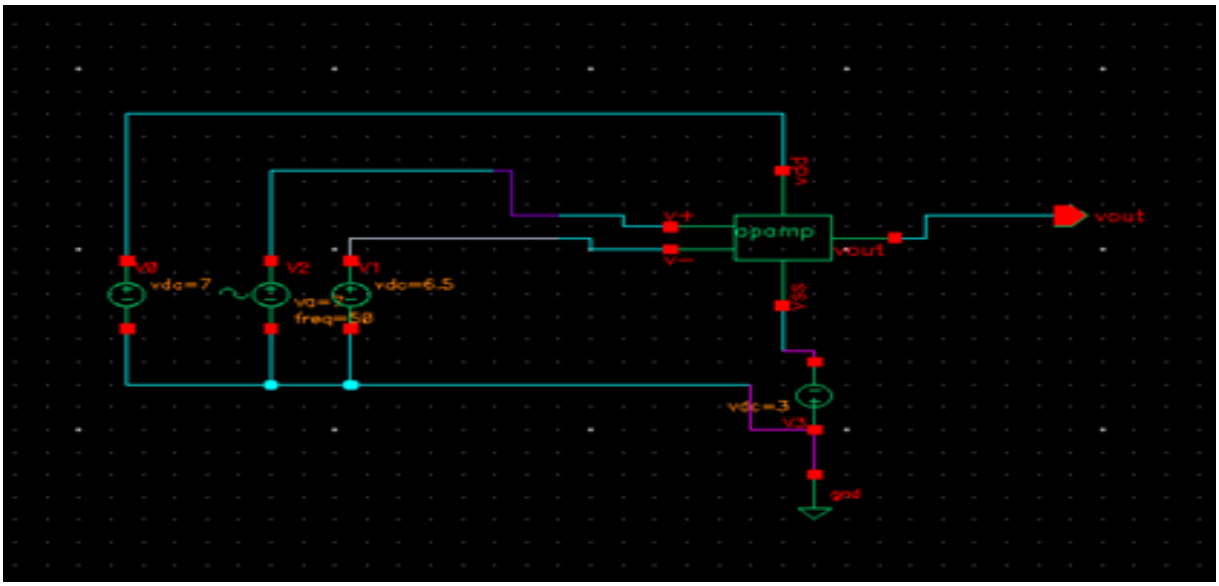

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Fig.5 Schematic diagram of Comparator using Op-amp

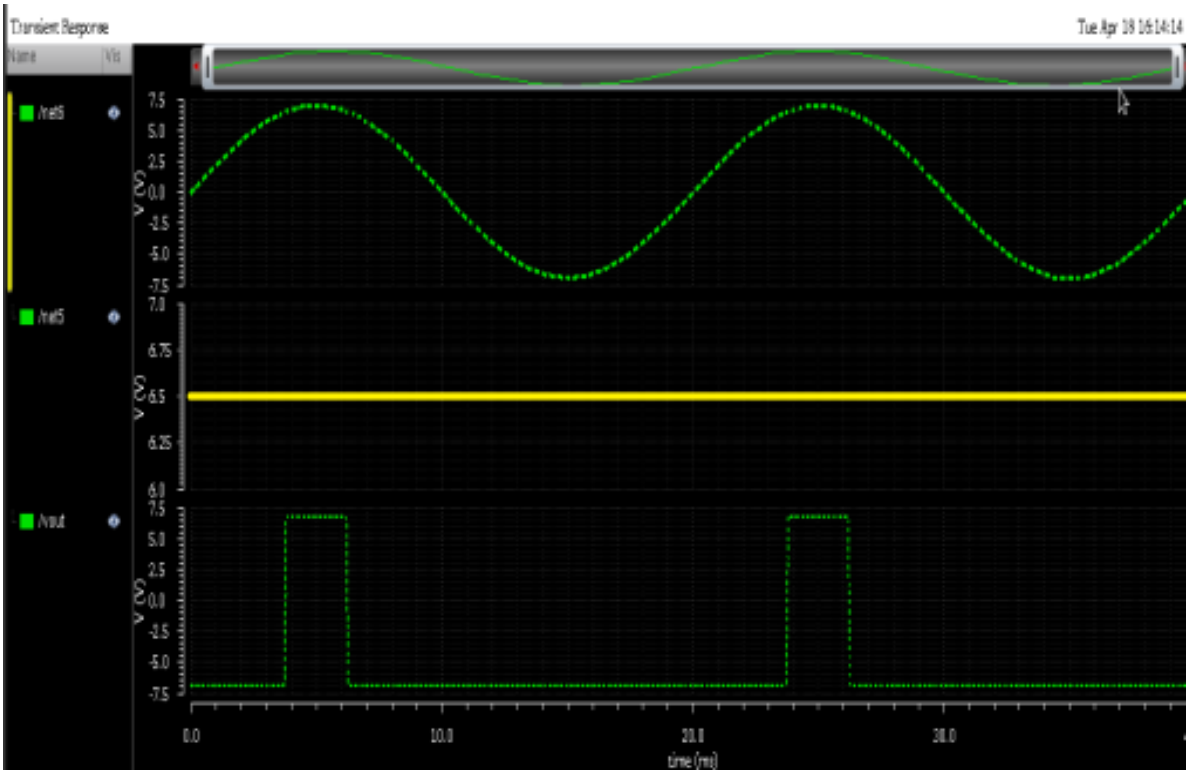

Fig.6 Output results of comparator

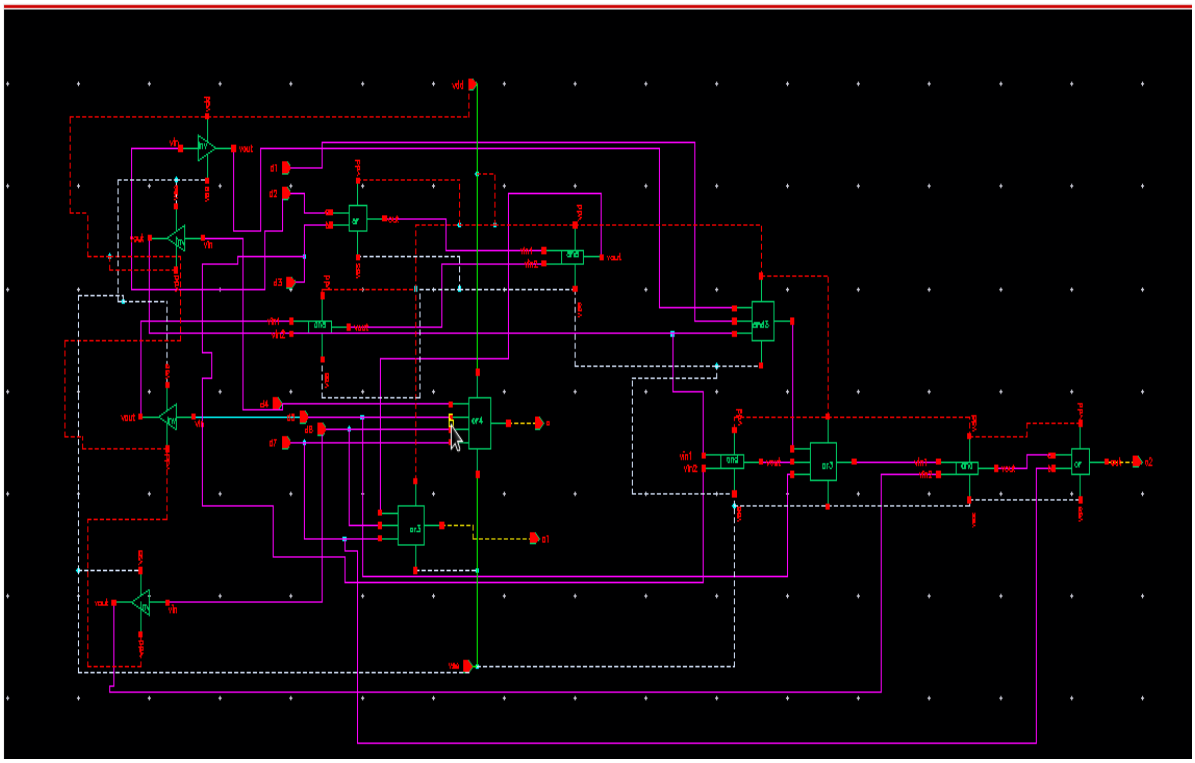

Fig.7Schematic diagram 8 to 3 priority encoder

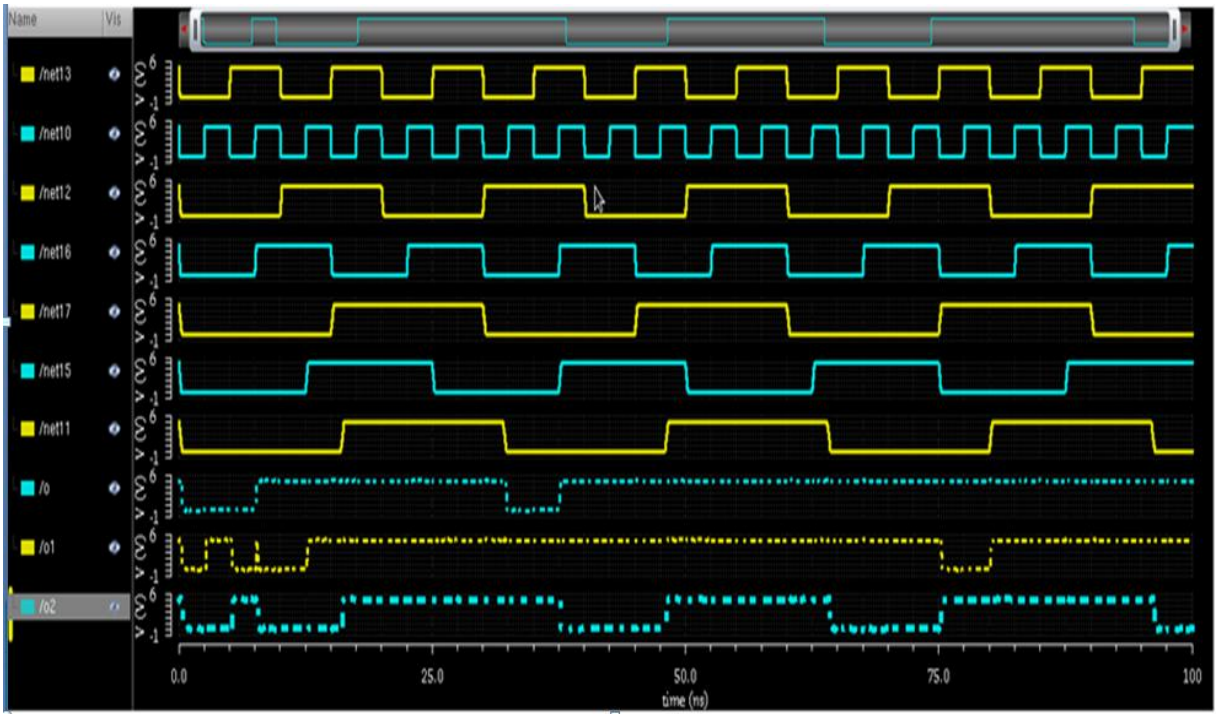

Fig.8.Results of 8x3 priority encoder

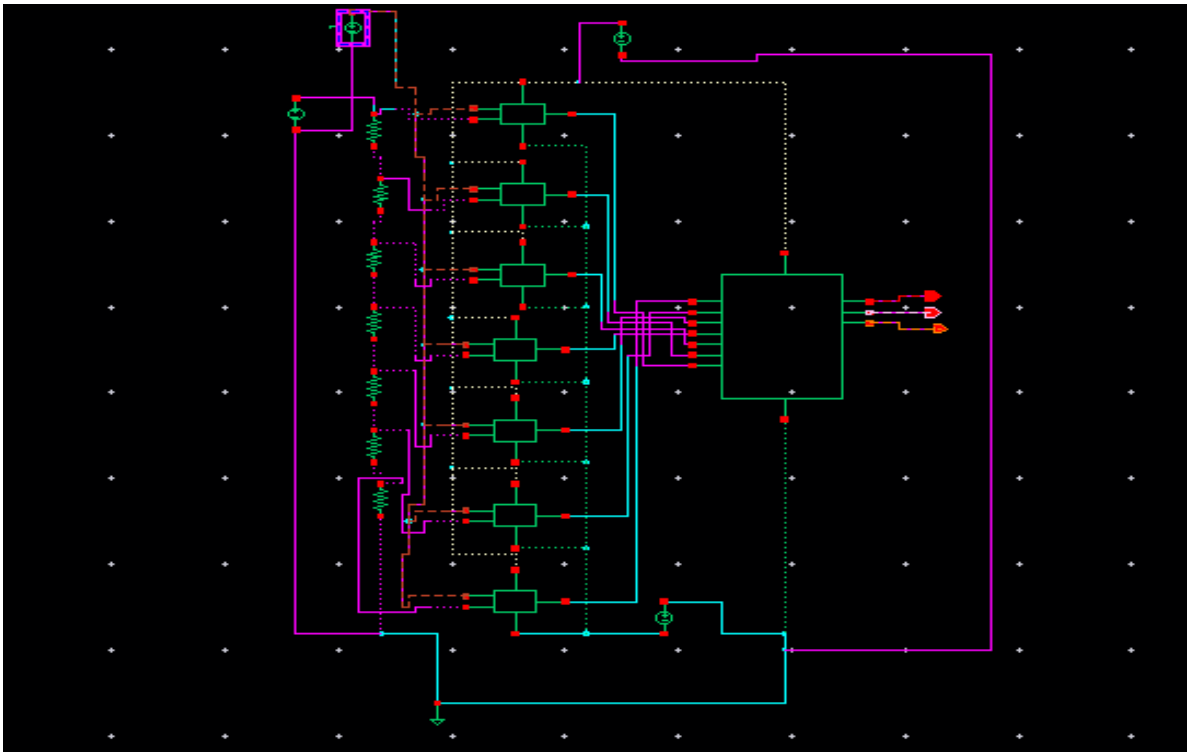

Fig.9 Schematic diagram of Flash ADC

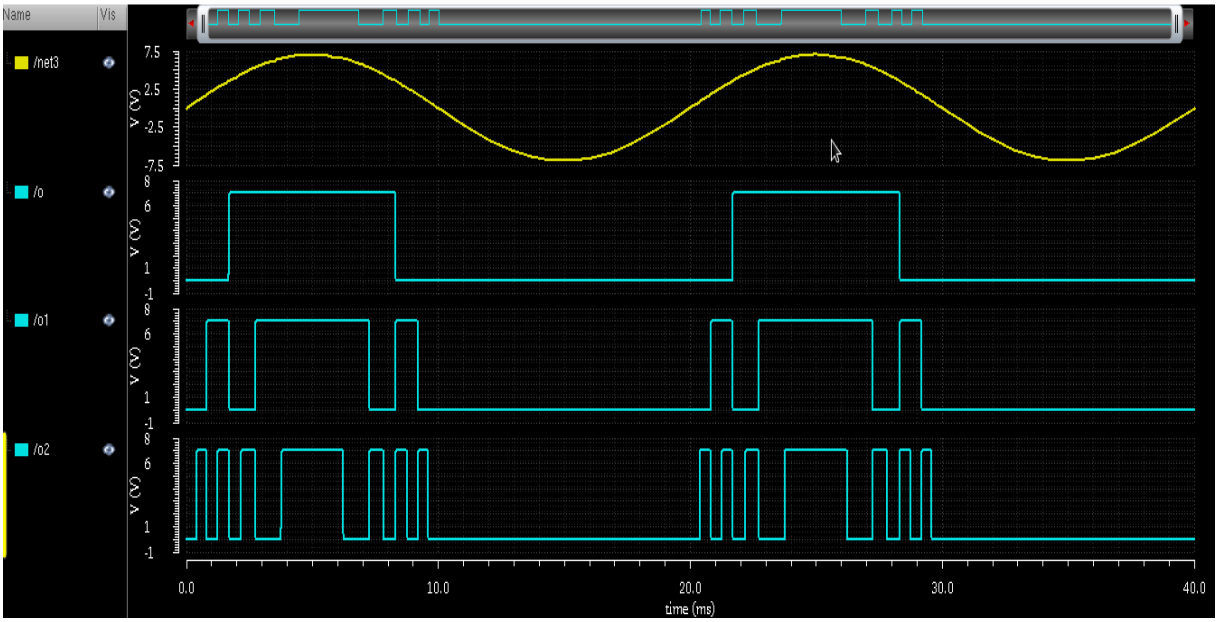

Fig.10. ADC output for analog i/p 7

TABLE I

COMPARISON OF POWER, DELAY AND PDP

parameter	**Comparator**	**Priority Encoder**	**Flash ADC**	**7**	**8**	**9**
Power (mw)	2.335	1.661	148.5	19.4	36.2	0.66
Delay (ps)	2.62 X10^{9}	267.6	191.8		1877	
Power delay product (pJ)	0.006	4.4	0.283			

The comparison of power consumption is slightly more compared with existing methods but delay is lesser than other methods. so it has high conversion speed compared with other methods.

Conclusion

. A simple and fast Flash ADC architecture that uses a Opamp comparator and an 8 to 3 priority encoder has been proposed. The circuit design and simulation results of 3-bit Flash ADC using 180nm technology have been presented using cadence. Flash ADC is power hungry and complex circuit, so it is a challenge to design and implement low power ADC with high speed applications. Moreover, the architecture of ADC can be extended from medium-to-high resolution applications because of the simplicity of the circuit and also the circuit should be portable to smaller feature size CMOS technologies with lower supply voltages.

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