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Design of Fast, Minimum Power Non-Volatile Master Slave Flip-Flop for Memory Storage

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Abstract:-Fast, energy-efficient, and compact memory solutions are becoming more and more necessary in the age of smart devices and the internet. The use of spintronics, an electron spin-based technology, in place for traditional charge-based semiconductor devices is one possible approach to reaching this aim. Spintronics makes it possible to transfer and store data and has the potential to significantly reduce power usage, ushering in the era of "green electronics." a junction in the magnetic tunnel (MTJ), This promise can be realized in practice, as in the case of a spintronic device that can be ruled by spin-orbit torques (SOTs). This device offers higher speed and energy efficiency because to magnetization that is parallel to the plane (PMTJ). A unique Non-Variable Master-Slave Flip-Flop (NVMSFF) design appropriate. A design of NVMSFF adopts a strategy by combining 45nm technology with a SOT-PMTJ circuit based on a Verilog-A model and utilising spintronics. The study also describes the creation and evaluation of 4x4 and 8x8 memory arrays using both the current NVSFF and the suggested NVMSFF. The findings show that the modified NVMSFF performs better than the conventional NVSFF in decreased delays, chip area usage, and power consumption. Additionally, smaller and more energy-efficient memory arrays have been created as a result of the proposed NVMSFF.

Keywords*: Spin Orbit Torque (SOT), Master Slave Flip Flop Non-Volatile (NVMSFF), Magnetic Tunnel Junction (MTJ), Spintronic, and Verilog-A Model.*

1. Introduction

In the rapidly evolving landscape of technology, there is an ever-increasing demand for digital systems capable of storing vast amounts of data. To meet this demand, a wide array of semiconductor memory technologies are being explored additionally, the demand for large amounts of data storage has sparked the creation of memory registers that employ cutting-edge, space-saving design principles. Magnetic Tunnel Junction (SOT-MTJ) of

Spin Orbit Torque, a sophisticated spintronic devices. This discovery offers the intriguing prospect of regulating the magnetic states inside a magnetic tunnel junction by use of spin-polarized current pulses. This capability has the potential to enhance density, speed, performance, and power efficiency in numerous real-time applications, including memory circuitry [2]–[4], logic circuits [5], and RF oscillators [6].Historically, magnetic tunnel junction devices have been configured with two terminals and have been controlled using mechanisms like spin transfer torque hybrid combination of VCMA and STT. However, the torque generated by spin-polarized current pulses aligned with the free layer's magnetization is inherently weak. Consequently, the free layer's magnetization accumulates energy slowly, leading to random switching over a broad range of switching times, typically on the order of a few nanoseconds [7].

In summary, the field of spintronic devices, particularly SOT-MTJs, holds significant promise in meeting the requirements of modern digital systems and extensive data storage. These devices, offering electrical control over magnetic states, have the potential to revolutionize memory technology, thereby enhancing performance and efficiency across various applications. Nevertheless, challenges such as switching speed and randomness must be addressed for these devices to realize their full potential. Traditional two-terminal magnetic tunnel junction (MTJ) devices encounter issues with slowness and energy inefficiency when subjected to current pulses due to ohmic losses. The spin transfer torque mechanism provides a solution for controlling the magnetic state of MTJ devices through current pulses that transfer spin angular momentum. However, it's vital to note that this mechanism is effective only when the pulse magnitude exceeds a specific current threshold for a corresponding duration. This approach can overcome the limitations of conventional MTJ devices, making them more energy-efficient and effective in various applications. Nevertheless, the current threshold for the spin transfer torque mechanism significantly increases as the pulse duration decreases. This high-speed operation can compromise energy efficiency, necessitating a high current density. The "incubation time" phenomenon is closely related to the spin transfer torque mechanism, which also contributes to the random magnetic tunnel junction switching (MTJ) devices over a wide range switching times [9].

The incubation period denotes how long it takes for the system to build up enough spin angular momentum—primarily from the Spin-polarized current was injected to initiate the switching process. A unpredictable behaviour of magnetic tunnel junction devices is further exacerbated by heat variations during magnetization, which have a major impact on the incubation time.

To sum up, challenges associated with the spin transfer torque mechanism include increased current thresholds for faster operation, potentially impacting energy efficiency, and the occurrence of random switching times due to the incubation time, influenced by thermal fluctuations. Addressing these challenges is crucial to advancing the performance and reliability of MTJ devices in spintronic applications.

In the realm of high-performance and low-power spintronic applications, there is a growing emphasis on devices for current-induced spin orbit torque, which is a prominent area of research [10-12]. These devices offer exciting possibilities for controlling magnetic tunnel junctions (MTJs) using spin orbit torque, especially in the context of three-terminal MTJs with perpendicular-to-the-plane magnetization (PMTJ). This approach provides high-speed operation and energy efficiency while enhancing reliability by isolating the read path from the write path [11-13]. In this configuration, the current in the write path does not traverse the tunnel barriers, reducing the risk of electric breakdowns. Additionally, the initial spin orbit torque is significant due to the nearly

orthogonal alignment of PMTJ devices. As a result, the free layer magnetization becomes energized rapidly after the application of a current pulse, with virtually no incubation time. This enables efficient and deterministic control of the devices using brief current pulses, typically lasting only a fraction of a nanosecond [10-11].To summarize, gadgets that create spin orbit torque from current, particularly these context of three-terminal PMTJ configurations, are attracting considerable attention in the pursuit of high-performance and energy-efficient spintronic applications. These devices offer advantages in terms of speed, reliability, and control, making them promising candidates for a wide range of emerging technologies.

The integration of a Model of the Spin Orbit Torque (SOT) - Magnetic Tunnel Junction (MTJ) apparatus utilising Verilog-A modelling is the primary emphasis of this work. To design a low-power D-flip flop for use in memory register designs with 45nm CMOS technology is the goal. By mixing CMOS and spintronic components, this strategy makes use of the principles of hybrid circuit methodology.

Researchers and technologists are drawn to Model of the Spin Orbit Torque -based memory circuits because of the non-volatile properties and energy efficiency [14–15]. These flip flops are therefore widely used in contemporary, effective applications [16–18]. The essay is set up like follows: Chapter II: This section presents Model of the Spin Orbit Torque (SOT) - Magnetic Tunnel Junction (MTJ) device model-based low-power D-flip flop designs that are both current and modified. Section III: Here, the design of memory registers is detailed, utilizing the D-flip flop introduced in Section II. Section IV: Simulation data and comparisons are provided in this section to give an understanding of how well the suggested designs work. Part V: This part wraps up the argument by summarising the results and outlining possible future lines of inquiry. In conclusion, this study demonstrates the use of SOT-MTJ devices, a type of Spintronic technology, in the development of non-volatile, low-power D-flip flops and memory registers. In the context of hybrid CMOS and Spintronic circuits, this strategy offers interesting opportunities for mixed-signal design and holds the potential to improve the effectiveness and performance of Non-Volatile SoC applications.

I. Using the Spin Orbit Torque (SOT) and Magnetic Tunnel Junction (MTJ) device concepts, a D-flip flop is designed.

A. A Magnetic Tunnel Junction Device (PMTJ) oriented perpendicular to Plane Magnetization

The Plane Magnetic Tunnel Junction (PMTJ) device model is implemented in Verilog-A in this study, which contrasts with the Verilog-A implementation of the device model [19]. This study primarily focuses on three-terminal PMTJ devices with current-driven spin orbit torque, paying close attention to their electrical, magnetic, and thermal properties. This PMTJ device model is noteworthy since it includes both field-type and damping-type spin orbit torque mechanisms. Furthermore, it provides an in-depth analysis of the device's thermal performance, accounting for temperature effects. As a result, the three-terminal PMTJ device may be precisely and effectively simulated using this all-encompassing device model, which takes into account both its electrical and magnetic properties.. A crucial feature of this model is its capacity to facilitate magnetic state switching within the device using spin orbit torques, a fundamental aspect for the operation and control of spintronic devices like the PMTJ, promising advantages in terms of performance and energy efficiency. In essence, this research incorporates a robust and versatile three-terminal PMTJ device model implemented in Verilog-A. This model facilitates a comprehensive analysis of the PMTJ device's electrical, magnetic, and thermal properties,

rendering it a valuable tool for simulating and comprehending the behavior of such devices, especially in the context of spin orbit torque-driven magnetic state switching.

The general structure of a three-terminal Figure 1 shows a parallel to the Plane Magnetization Magnetic Tunnel Junction (PMTJ) gadget. A tunnelling barrier separates the two ferromagnetic (FM) layers, which is the typical structure. Typically, a thick metal layer known as the channel is placed on top of this tunnelling barrier. The first FM layer, with its magnetization aligned along the e_z direction, is known as the reference layer (RL). The free layer, or FL, is the second FM layer and can be oriented either anti-parallel (AP) or parallel (P) to the reference layer's magnetization. By use of mechanisms involving current-induced spin orbit torque, the magnetization of the free layer is directed in this way. Visualisation of the dynamic change in the free layer's magnetization direction at each time step in Figure 2. This change can be quantified by means of a unit vector, denoted as r̂, aligning with free layer's magnetization direction. This vector exhibits an angle θ relative to the e_z direction, while the plane formed by r̂ and the e_z direction is inclined at an angle φ concerning the e_x direction. Additionally, an externally applied magnetic field, represented as H_ext, is employed to support and influence the spin orbit torques acting on the system. In brief, the PMTJ device comprises two FM layers separated by a tunnelling barrier, with the manipulation of the free layer's magnetization orientation achieved through current-induced spin orbit torques. The angles θ and φ, in conjunction with the external magnetic field H_ext, are pivotal factors in determining the behavior and functionality of this spintronic device.

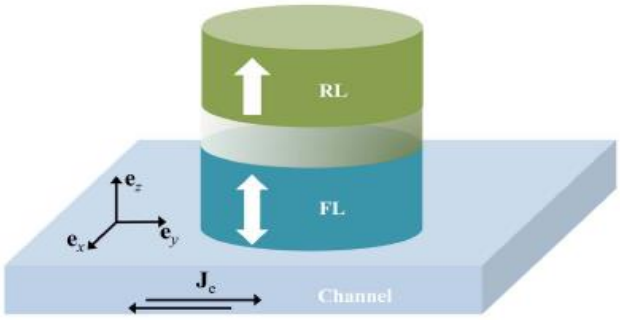

Fig. 1: The three terminals of the PMTJ device's general structure

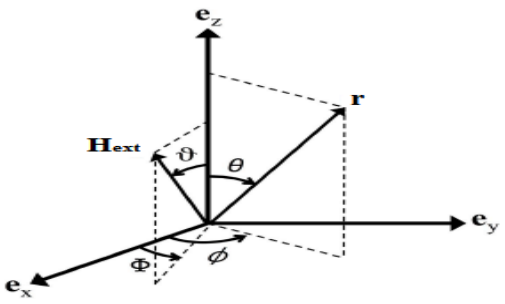

Figure 2: Magnetization of the free layer and an external magnetic field.

The time-dependent change in the magnetization of the free layer is typically described by the Landau-Lifshitz-Gilbert (LLG) Slonczewskiequation.. [18], given by equation (1):

$$dM/dt = -\gamma M \, x \, Heff + \alpha M \, x \, dM/dt + \tau$$

In this context, several critical variables and terms play a central role:

- **M (Magnetization of the Free Layer): This denotes how magnetic field of the free layer is aligned and oriented.**
- **$_{Heff}$ (Effective Magnetic Field):** The $_{Heff}$ refers to the magnetic field that is actually acting to make the free layer magnetic. It exerts a crucial influence on the system's behaviour..
- **t (Time):** Time, often denoted as 't,' is an essential parameter as it marks the progression and duration of events within the system.
- **γ (Gyro-Magnetic Ratio):** The gyro-magnetic ratio, symbolized by 'γ,' is a fundamental constant associated with the intrinsic properties of magnetic materials. It influences the response of the system to external influences.
- **α (Gilbert Damping Factor):** The α factor, known as the Gilbert damping factor, quantifies the rate at which the magnetization of a free layer reacts to outside forces. It displays how dissipative the system is.
- **τ (Spin Orbit Torque):** The τ term, encompassing both field-type and damping-type spin orbit torques, plays a crucial role in imparting torques to the system, which in turn affects the orientation

The estimation of the magnetic field's effectiveness an important feature of this system is H_{eff}, which involves ideas similar to magnetic anisotropy and Zeeman energy. As illustrated in equation (2):

$$Heff = -\mu_0 * Ms * Hext - Keff * M$$

In equation (2):

The permeability of empty space is - 0.

- Ms: The magnetization's saturation.

- H_ext: The magnetic field outside.

The effective anisotropy constant is $_{K\_eff.}$

.Equation (3) represents the temperature-dependent perpendicular-to-plane anisotropic magnetic field,$_{Hpp(T)}$

$_{Hpp(T)} = _{K\_pp} * M\_s * (1 - T/T\_C)$

In equation (3):

- $_{K\_pp}$: The perpendicular magnetic anisotropy constant.

- $_{T\_C.}$ The Curie temperature.

The magnetization 'M' is calculated using equation (4):

M = M_s * m

In equation (4), 'm' represents the unit vector of the magnetization direction.

In a three-terminal parallel to the Plane Magnetization Magnetic Tunnel Junction (PMTJ) gadget, these equations collectively give a mathematical framework to understand the dynamic behaviour of the magnetization of the free layer in response to different magnetic and thermal conditions.

$$\frac{dm}{dt} = -(\rho * m)\, X\, H_{eff} + (\xi * m)\, X\, \frac{dm}{dt} + \rho * \tau \quad (1)$$

$$H_{eff} = -\nabla_m \left\{ \frac{1}{2} * H_{pp}(T) * m_z^2 - m.(H_{ext} + H_L + H_{RL}) \right\} \quad (2)$$

$$H_{pp}(T) = \left\{ 2 * \frac{A_m(T)}{M_{sat}(T)} - 4 * \pi * M_{sat}(T) \right\} \quad (3)$$

$$m = (\cos(\theta), \sin(\emptyset)\sin(\theta), \cos(\emptyset)\sin(\theta)) \quad (4)$$

- M_sat (T) **(Saturated Magnetization):**M_sat, which is temperature-dependent (T), signifies the maximum achievable magnetization in the system.

- **A_m (Magnetic Anisotropy):**A_m, also temperature-dependent (T), characterizes the magnetic anisotropy of the system. It relates to the preferred magnetization direction within the material.

- **H_ext (External Magnetic Field):**H_ext represents an externally applied magnetic field necessary to support the generation of spin orbit torques within the system.

- **H_RL (Magnetic Field from the Reference Layer):** H_RL denotes the magnetic the reference layer's field, which adds to the overall magnetic dynamics.

- **H_L (Langevin Random Magnetic Field):** H_L reflects the effect of non-zero temperature on the cyclical variations in the accounts for Langevin random magnetic field [21–22]. H_L has components in each of the three spatial dimensions and is generated randomly using a Gaussian process with a mean value of zero.A generic resistive T network can be used to represent Magnetization in the plane perpendicular to Magnetic Tunnel Junction in reaction to different magnetic (PMTJ) device in an electrical circuit, as shown in Figure 3. This illustration shows:

- **GC (Channel Conductance):** GC characterizes the conductance within the channel segment of the device.

- **GT (Tunnelling Conductance):** GT pertains to the tunnelling conductance associated with the specific magnetic stack under consideration.

- **G (Overall Conductance):** G is a composite term encompassing two key components: a) **GS1 (Spin-Dependent Conductance):** GS1 represents the conductance that depends on spin orientation, a result of the relationship between temperature (T), applied voltage (V), and the PMTJ's magnetic response, particularly the angles θ and φ ,which characterise the orientations of the free layer and reference layer magnetizations..

- b) **GS2 (Spin-Independent Conductance):** GS2 is the conductance that remains unaffected by spin orientation.

The conductance term reliant on spin, **GS1**, exhibits sensitivity to temperature, voltage, and the magnetic behavior of the PMTJ. This sensitivity is further scrutinized through the tunnelling magneto-resistance (TMR) model, as expounded in [24-25]. The influence of voltage variations on **GS1** is articulated using the Brinkman model, as discussed in [26]. Additionally, the effects of temperature fluctuations on both **GS1** and **GS2** are captured by the Stratton model, as elaborated in [27].

The aggregate tunnelling conductance, **GT**, characterizing the PMTJ device, is subsequently expressed using equations (5) and (6).

In summary, this electrical circuit represents a thorough comprehension framework and modelingbehavior of PMTJ device, taking into account various factors such as temperature, voltage, and the magnetic configuration of the device. These models and equations are essential for analyzing and predicting the electrical characteristics of the PMTJ in different operating conditions.

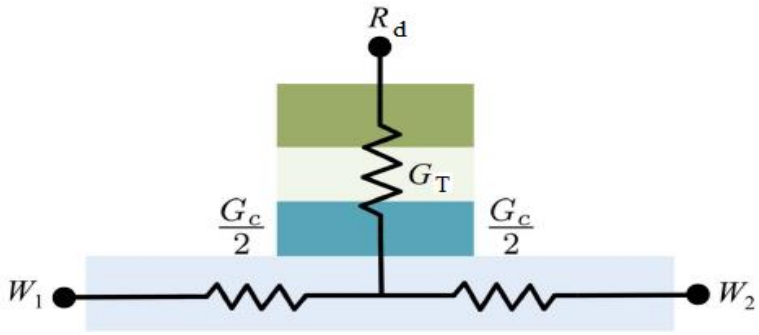

Fig. 3. A resistive T-Network-provided electrical circuit with three terminals for the PMTJ

$$G_T = G_{S1} + G_{S2} \quad (5)$$

$$G_T = G_0 * \frac{\propto T}{\sin(\propto T)}[2 + TMR(1 + \cos(\theta))] \sum_{i=0}^{2} C_i * V^i + P * T^{4/3} \quad (6)$$

Certainly, let's include the equations for the tunneling conductance and channel conductance you've mentioned:The tunnelling conductance, denoted as **GT**, for the PMTJ device can be expressed using equations (5) and (6) as shown below:

GT = G0 * exp(-α * TMR / T) [Equation 5]

In this equation:

- • **G0:** Represents the tunnelling conductance in a certain set of circumstances, specifically when a parallel setup is taken into account, at zero voltage bias and zero temperature.
- **α:** a variable based on the substance influencing the behavior of the device.
- **TMR (Tunnelling Magneto-Resistance):** This factor quantifies the magneto-resistance properties of the device, reflecting the impact of magnetic orientation on its conductance.

- **T (Temperature):** The temperature at which the device operates, influencing its conductance characteristics.
- **P:** A fitting parameter used to adjust and fine-tune the conductance behavior of the device.

This equation encapsulates the interplay of these parameters in determining the tunnelling conductance of the PMTJ device.

The channel conductance, **GC**, is described by equation (7):

GC = σc * (w / h) * (V / l) [Equation 7]

Where:

- σc: Channel conductivity.

- w: The channel's width.

- h: The channel's height.

- l: The channel's length.

-V:Voltage bias.

These equations together provide a comprehensive understanding of the tunneling conductance and channel conductance in the context of the PMTJ device. They take into account material-dependent parameters, temperature, voltage bias, and device geometry, allowing for the analysis of the electrical characteristics and behavior of the PMTJ under various conditions.

$$G_C = \sigma_c * \frac{w * h}{l} \qquad (7)$$

Indeed, Joule heating is an important factor to consider in the analysis of the device as it can affect the conductance and temperature of the PMTJ. Here's the equation representing the heating effect due to current flow:

The temperature increase, ΔT, owing to the Joule heating effect, is given by equation (8):

ΔT = (J^2 * R) / (σc * w * h) [Equation 8]

Where:

- ΔT: Temperature increase due to Joule heating.

- J: Current density.

- R: Resistance of the channel.

- σc: the conductivity of a channel..

- w: The channel's width.

- h: The channel's height.

This equation quantifies how the device's temperature increases as a result of the power dissipation due to the nonzero resistance in the channel when current flows through it. Understanding this temperature increase is crucial for accurately calculating the conductance and effective field of the PMTJ device, taking into account the effects of Joule heating and temperature variations.

$$T = T_o + R * |J_A|^2 \qquad (8)$$

Certainly, let's include the additional information regarding the temperature increase and the use of the Spectre tool by Cadence for evaluating the model under different modes of operation:

In equation (8), where ΔT represents the temperature increase due to Joule heating:

ΔT = (J^2 * R) / (σc * w * h) [Equation 8]

- T_o: Temperature at null current density.

- J_A: Current density.

- R: Rate of heating.

The Spectre tool provided by Cadence is employed to assess the presented model with three different modes of operation:

1. Liberal Mode: This mode might prioritize speed and efficiency, potentially sacrificing some level of accuracy in the simulation.

2. Moderate Mode: This mode likely offers a balanced trade-off between accuracy and computational time, providing reasonably accurate results while maintaining efficiency.

3. Conservative Mode: Shifting towards the conservative mode of operation aims to achieve superior accuracy and device efficiency, even if it requires slightly increased computational time.

The mode selection is based on the particular simulation requirements and desired level of accuracy..It's a trade-off between accuracy and computational resources. Adjusting the mode of operation allows engineers and researchers to tailor the simulation to their needs, ensuring that they obtain the most relevant and reliable results for their analysis of the PMTJ device.

B. The current Non-Volatile Master Slave Flip Flop (NVMSFF) protocol [30]

Figure 4 illustrates strategic incorporation of three-terminal as a standard the master-slave flip-flop is CMOS-based., fulfilling its primary roles in data storage and processing. However, when the system shifts into backup mode or enters sleep mode, effectively disabling the power gating circuitry, retains the logical state stored within the PMTJ device. This data retention ensures a seamless data transition when operation is subsequently reactivated, with the power gating circuitry resuming its regular functions. Figure 4 offers an illustrative depiction of this integration strategy. Two basic parts make up the NVMSFF circuit, as shown in Figure 4: a volatile master latch and a non-volatile slave latch. The non-volatile slave latch is built using two PMTJ devices (PMTJ1 and PMTJ2), whereas the volatile master latch uses simple CMOS circuitry. These PMTJ devices,

which are essential for maintaining latched data even when the electricity is turned off., are accessed by the corresponding NMOS transistors, which make up the circuit's non-volatile portion.

The current NVMSFF's schematic circuit was created using Cadence tools. Is shown in Figure 5, which illustrates the circuit's physical layout. Figure 6 offers a thorough timing diagram to further explain the operational modes and transitions. Various operational modes, are illustrated in this diagram. Contingent upon states of signals B, E, and R. During active mode operation, signal E is consistently maintained at a high logic level, while signals R and E are set to low logic levels. The low state of signal R effectively deactivates NMOS devices, rendering the PMTJ devices inaccessible and preserving the stored logical state. This innovative integration of PMTJ devices with CMOS flip-flops represents a robust solution for ensuring data retention and stability during power transitions and non-operational phases. It holds significant promise for non-volatile memory applications, guaranteeing data integrity even in challenging conditions.

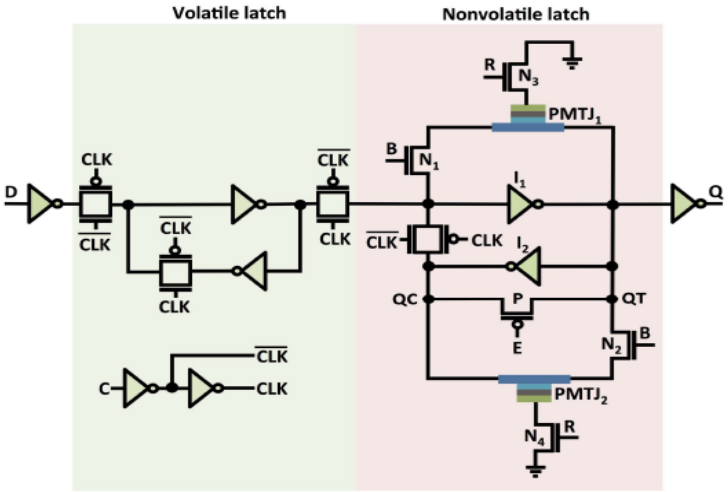

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Fig. 4. Non-Volatile Master Slave Flip-Flop (NVMSFF) Circuit Based on Existing Volatile Master Latch and Non-Volatile Slave Latch.

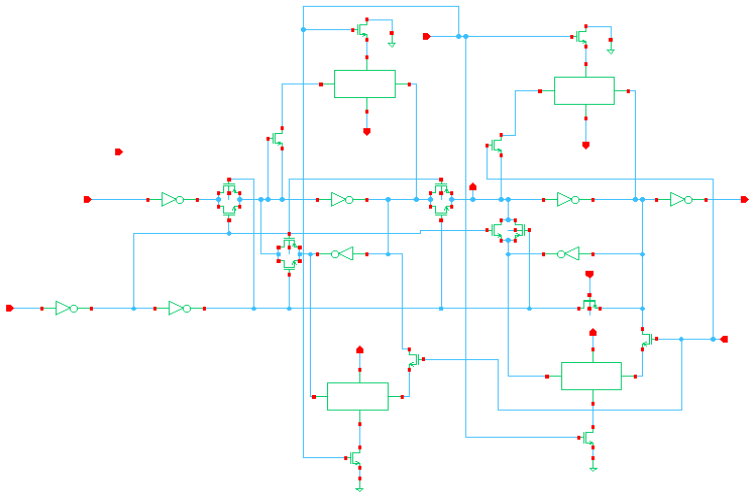

Fig. 5. Schematic Circuit for Non-Variable Master Slave Flip-Flop (NVMSFF)

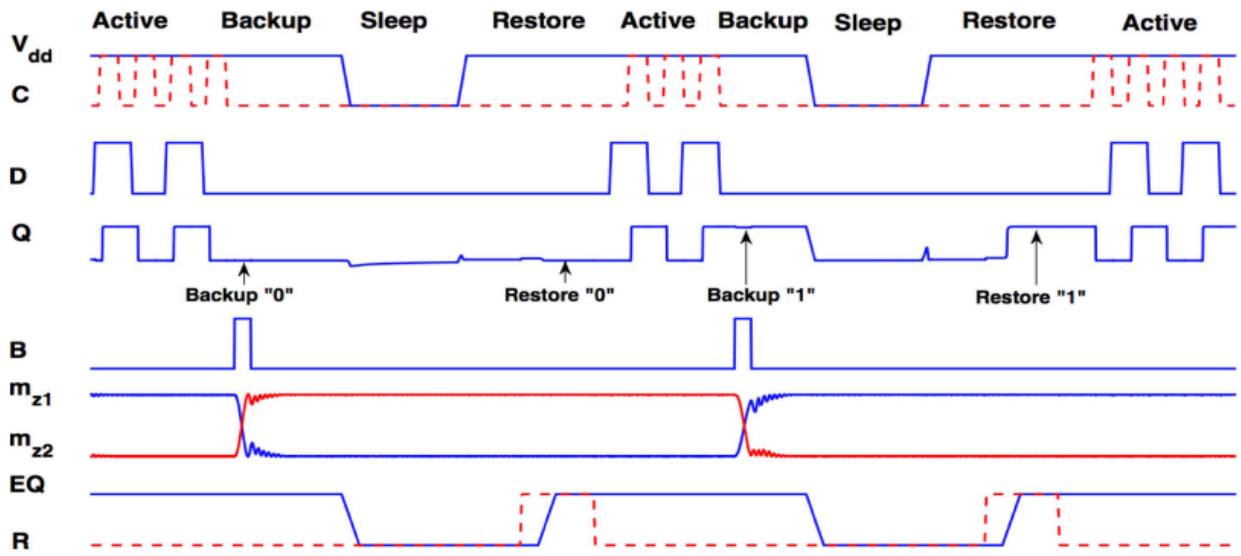

Fig.-6. Current Timing Diagram for Non-Volatile Master Slave Flip-Flop (NVMSFF)

A specific technique is carried out to ensure the preservation of the data present in the Perpendicular to the Plane Magnetization Magnetic Tunnel Junction before disconnecting the power supply gating network. (PMTJ) device:

1. A high logic level is selected for Signal B.

2. A low logic level of Signal C is maintained.

A current path is created through both PMTJ devices' channels under these circumstances as a result of the voltage differential that develops at QT and QC nodes. The flow of currents through these PMTJ devices is controlled by the logical states of nodes QT and QC. As well as modifications in the magnetization of the free layers in both devices.

The ability of each PMTJ device to permit current flow is essential in deciding the circuit's following restoration mode of operation. The maintenance of signals E and C at low logic levels further supports mode.
In essence, the aim of keeping signal B at a high level and signal C at a low level is to create a backup of the data held in the PMTJ device. Across this configuration, current can flow across the devices, changing their internal magnetization states. It is crucial for the circuit's restoration mode of operation, which afterwards ensures data integrity when the Network power supply gating is disabled, to be able to control these states through the flow of current.

C.Non-Volatile Master Slave Flip Flop with Modifications (NVMSFF)

When compared to current the proposed improvement to the Non-Volatile Master-Slave Flip-Flop (NVMSFF) circuit, non-volatile master-slave flip-flop configurations, is based on a hybrid design that combines Spintronic and CMOS elements, is notable for its notable reduction in the number of transistor devices. The circuit is made simpler and has a smaller footprint as a result of the decreased device count.

The proposed circuit's device count is briefly broken down as follows:

- CMOS inverters: seven there are 7 PMOS devices and 7 NMOS devices in this set.
- 2 SOT-PMTJ devices: These Spintronic components play a critical role in non-volatile storage and data retention.

The streamlined use of devices in the proposed circuit translates into a more efficient use of space. Figure 7 offers a visual representation of the proposed modified NVMSFF circuit, realized through the utilization of Cadence tools.This innovative design approach, characterized by a reduced device count, promises benefits in terms of both area efficiency and power consumption. It stands as a promising solution for diverse applications that call for non-volatile memory elements while striving for optimal space utilization.

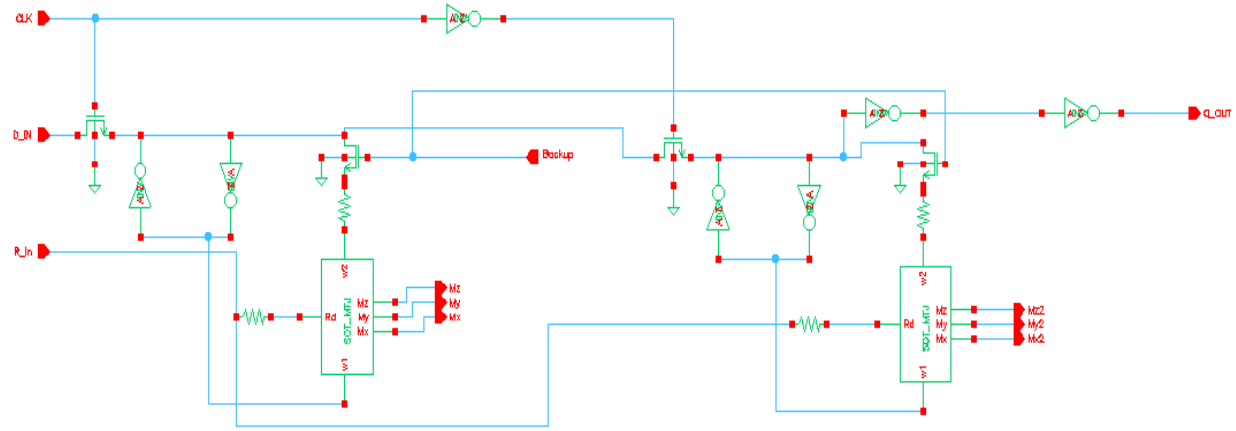

Fig.-7. Proposed Non-Volatile Master Slave Flip-Flop Circuit Schematic is modified.

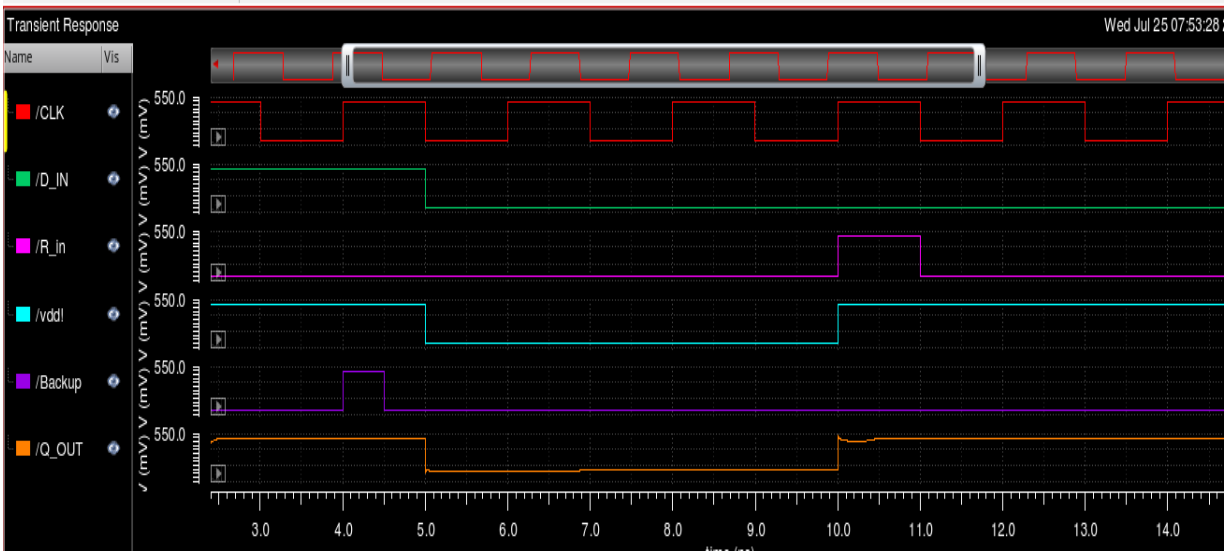

Fig.-8. the proposed modified flip-flop non-volatile master slave's simulation results

The proposed modification to the NVMSFF, short for Non-Volatile Master-Slave Flip-Flop circuit is a clever design that effectively operates during both phases of the clock signal, making use of two separate NMOS devices for this dual-phase functionality. This approach enables efficient data storage and retrieval in the following manner:

1. **Positive Clock Cycle**: During the positive clock cycle, the circuit engages the volatile master latch section. This phase is dedicated to capturing and securely latching the data.

2. **Negative Clock Cycle**: In contrast, during the negative clock cycle, the circuit's non-volatile slave latch part takes control. Here, data is stored for a long time by being preserved in a non-volatile manner using Spintronic components.

As shown in Figure 8, the Backup signal's logic values govern whether the circuit works in active mode or backup mode. The power supply gating network is cut off from the circuit when the Backup signal is activated, allowing the Spintronic Magnetic Tunnel Junction (SOT-PMTJ) device to store data. The data that was previously saved during when the power supply gating network is activated, turning on the Read signal once more successfully returns the latch to the backup state is subsequently reactivated. This dual-mode operational framework serves a dual purpose: it ensures data retention during power transitions and facilitates data restoration when the power supply is reinstated. In doing so, it guarantees data integrity and non-volatility, making it a robust solution for critical applications.

2. Register Memory Design Using NVMSFF

A group of cells together referred to as a "bit cell" is a key building block in the field of memory construction these collections of cells hold sets of bits, referred to as "words," that represent different 0s and 1s combinations. Flip-flops are frequently used in memory architectures to represent memory words; one bit of information can be stored in each flip-flop.

Typically, each bit cell had three important inputs:

1. The conduit for data that is either stored inside the cell or retrieved from it is provided by this input.

2. Cell Select Line: This line is crucial in determining which flip-flop or bit cell will be used in the memory array.

3.The Read/Write Select Signal is essential in distinguishing whether a memory bit cell is in the read (for data retrieval) or write (for data storing) modes of operation.

An N*N register memory's logical architecture is made up of binary cells with N bits and N words. A 2x2 memory architecture, for instance, consists of 2-bit binary cells arranged in a 2x2 grid. You would need N log2(N) x N decoders, N2 the N:1 multiplexer, with memory bit cells circuits to create a NxN memory architecture. In your work, 4x4 and 8x8 memory arrays have been designed using the low-power Non-Volatile Master-Slave Flip-Flop (NVMSFF) which has suggested. Read, write, and hold operations that are similar to those in Random Access Memory (RAM) arrays have been analogously executed in a variety of operational modes, including active mode, backup mode, and sleep mode.

In a previous section, it was detailed how these various operational modes affect bit cells or flip-flops. Figures 10 and 11 show schematic designs of the 4x4 and 8x8 memory array architectures, which were painstakingly created using the Cadence Virtuoso Schematic Design tool. The physical configuration of the memory cells and their connections within the memory architecture are physically represented by these memory arrays.

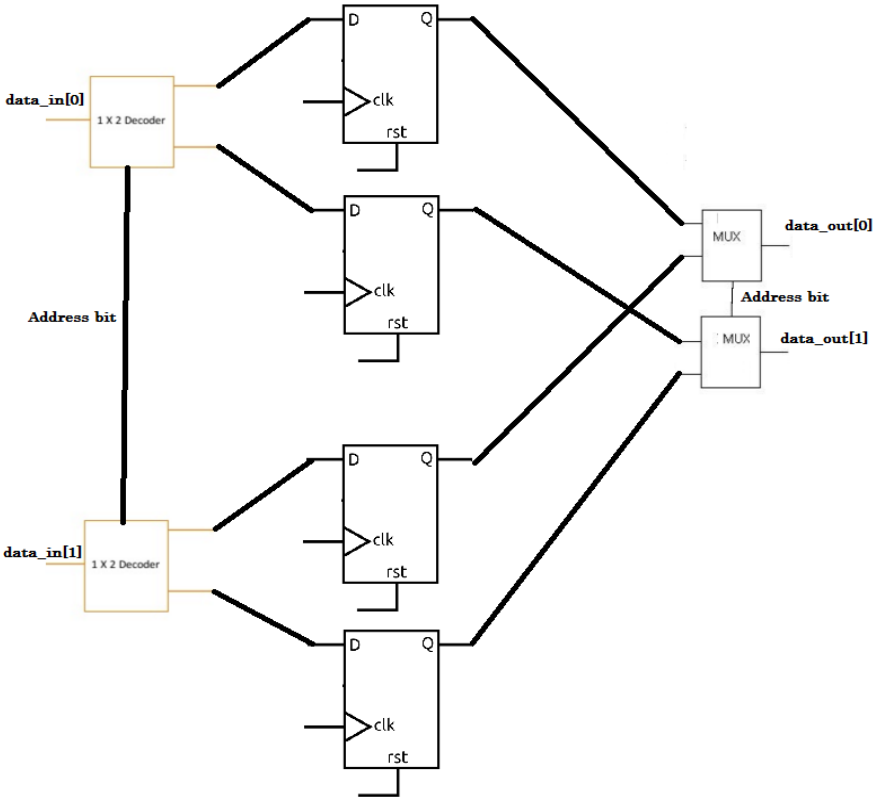

Fig.-9. General 2x2 Memory Architecture

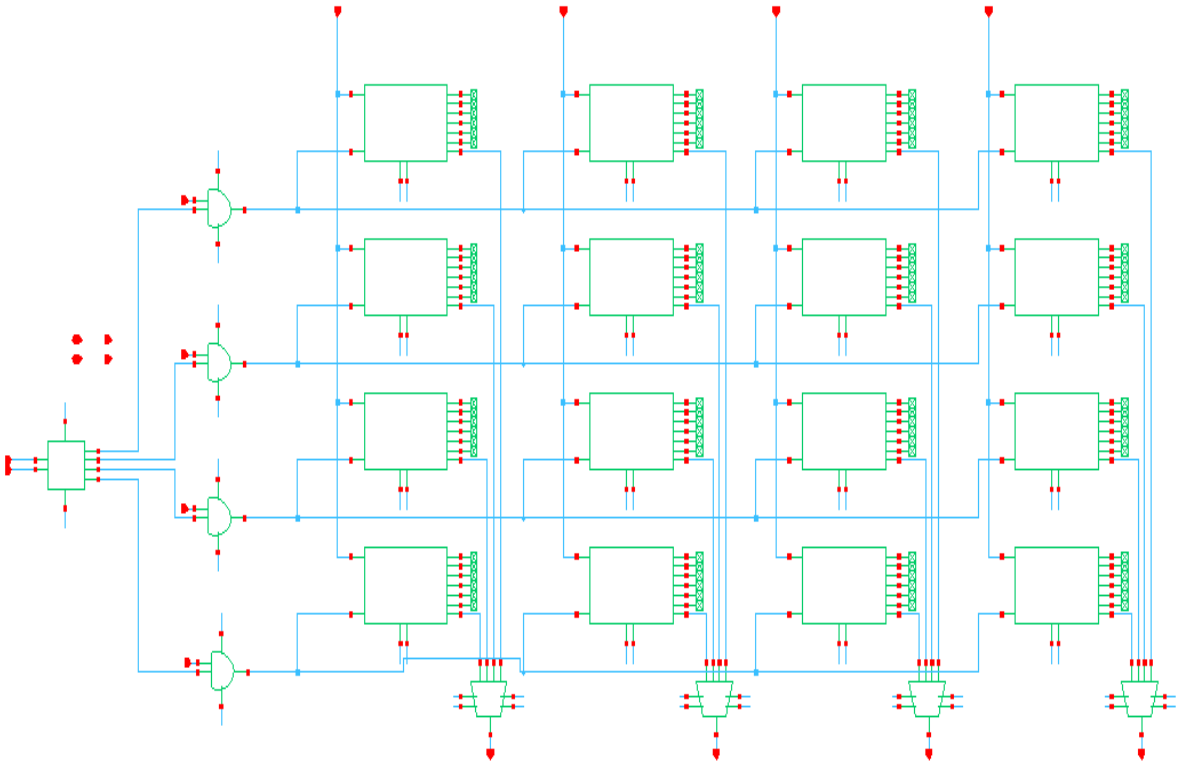

Fig.-10. ArchitectureModified NVMSFF 4x4 Memory Array Architecture Being Proposed

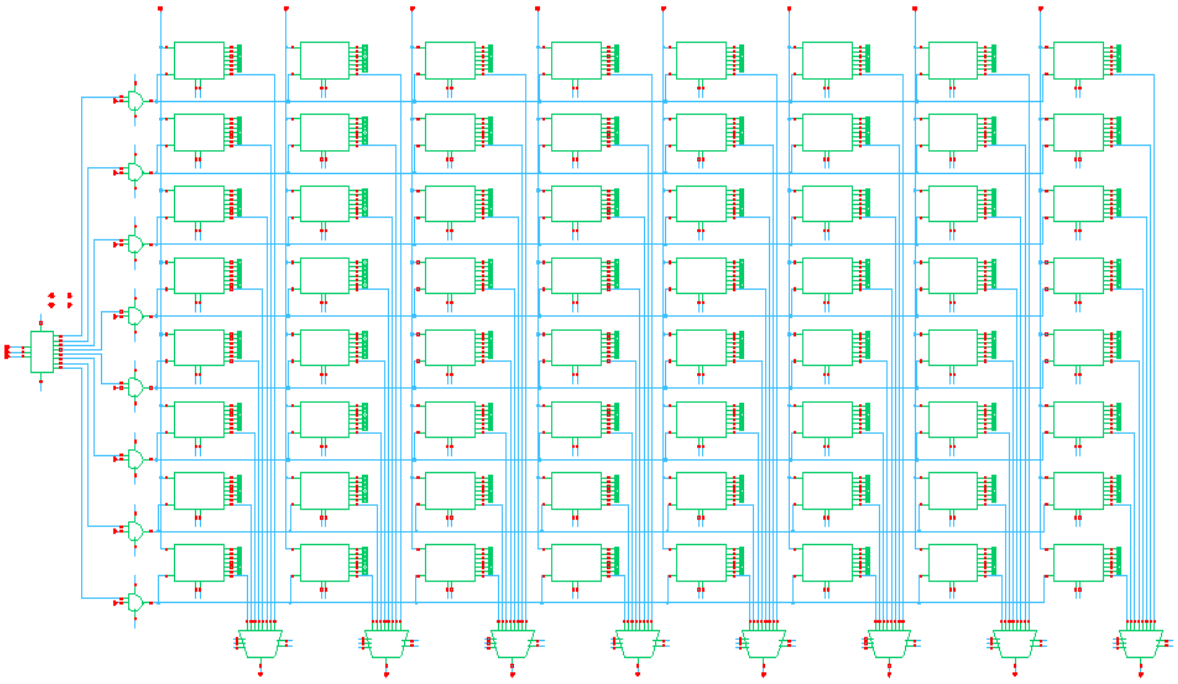

Fig.-11. utilizing a modified NVMSFF, memory array of an 8x8.

3. Results And Analysis

The research conducted in this study effectively utilized Cadence Virtuoso Tools in conjunction with 45nm CMOS process technology. Circuit simulations were carried out using the Cadence Spectre tool, an integral part of the Cadence Virtuoso Analog Design Environment (ADE). Notably, In order to create a hybrid device model that seamlessly incorporates both CMOS and Spintronic components, the Spintronic device SOT-PMTJ was built through a Verilog-A model. The results of transient response simulations for a 4x4 memory array, painstakingly created utilising both the current NVMSFF circuit and the proposed improved low-power NVMSFF, are vividly displayed in Figures 11 and 12, respectively. These simulation results unequivocally demonstrate the higher performance of the array which creates NVMSFF modified, a low-power device that has been suggested. It particularly shines in terms of data output and logic level strength. Additionally, thorough analyses included other essential factors including power usage, delay, and space. An in-depth investigation of the transient response simulation results for an 8x8 memory array was also carried out, reiterating the trend of higher performance shown by the memory array created with the proposed modified low-power NVMSFF. This performance gain, particularly in terms of data output and logic level strength, highlights the potential advantages and benefits provided by the improved array architecture. These simulation results offer compelling proof of its efficiency and capacity to improve performance and data dependability.

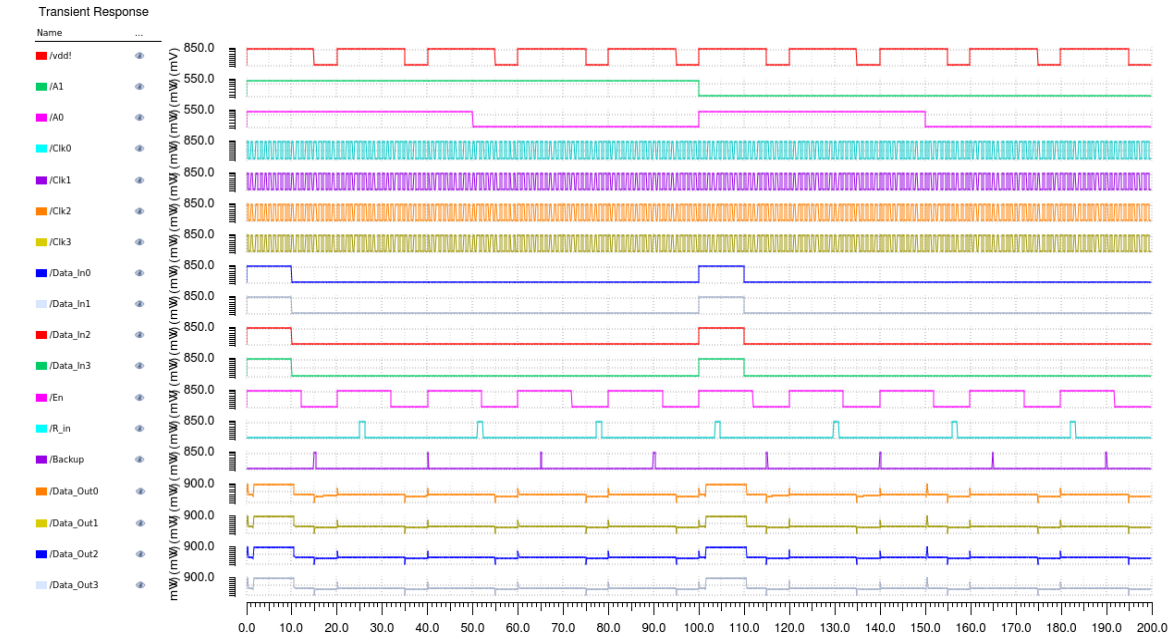

Fig.-12. using the current NVMSFF, transient analysis simulation for the 4x4 architecture

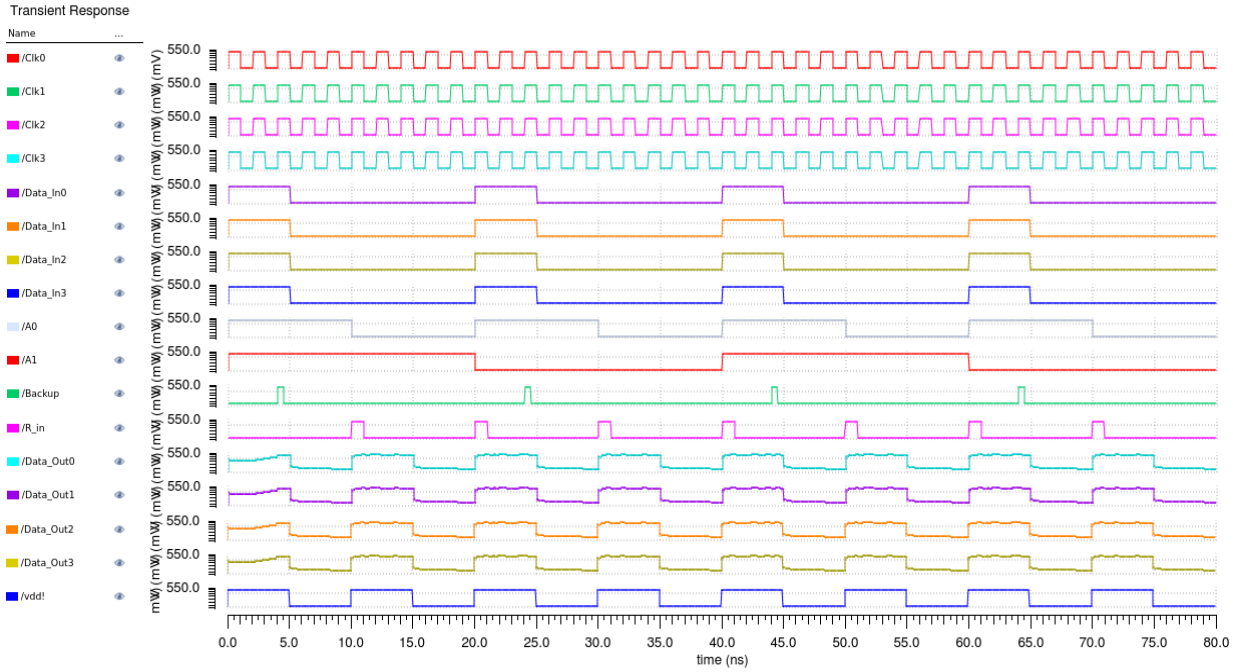

Fig.-13Making use of the suggested Modified Low Power NVMSFF, transient analysis simulation for the 4x4 Memory Array Architecture is performed.

Table I. Simulation Setup Parameters

Parameters	**Descriptions**
Technology	CMOS 45 nm
Tool Used	Cadence Virtuoso ADE

Spin Transistor	SOT-PMTJ (Verilog-A Model)
Simulator	Spectre
Input Supply Voltage	0.5V
Simulation Temperature	Room Temperature (27 °C)

Table II. Flip-Flop Performance Comparison and Analysis

Performance Parameter	**Existing NVMSFF [30]**	**Proposed Modified NVMSFF**
Average Power Consumption (µW)	1.935 µW	0.178 µW
Time Delay (ns)	1.175 ns	0.384 ns
Power-Delay Product (fJ)	2.2736 fJ	0.06835 fJ
No of Inverters	8	7
No of MOS Devices	12	4
No of SOT-PMTJ	2	2

The general settings for the simulation used in this study are summarised in Table-I. Additionally, Table-II provides a thorough examination of the performance differences between the proposed improved low-power NVMSFF and the current NVMSFF. This comparative table clearly demonstrates the significant benefits of the improved NVMSFF over the current NVMSFF in terms of a number of important factors, such as transistors, power consumption, delay, and the number of devices. Due to the more effective use of transistors and inverters, the suggested improved NVMSFF circuit exhibits an approximately 44% size decrease, making it an area-efficient solution.

A comparative PVT (Process, Voltage, and Temperature) based temperature study is also included in Table-III, with a particular emphasis on the overall power consumption for the two types of NVMSFF circuits. This thorough investigation confirms that the improved NVMSFF, when compared to the original NVMSFF, is superior throughout a wide range of semiconductor device operating temperatures. The use of silicon in different semiconductor applications is further enhanced by this superiority. Additionally, a thorough analysis of original NVMSFF circuit as well as the suggested circuit has been conducted. The results are graphically represented in Figure 13. The suggested improved NVMSFF demonstrates negligible sensitivity to temperature variations, in contrast to the conventional NVMSFF circuit, which exhibits a significant fluctuation in total power usage with rising temperature. These findings underscore the robustness and stability of the proposed modified NVMSFF circuit, particularly under varying temperature conditions, making it a highly reliable choice for diverse semiconductor applications.

Table III. Comparative temperature analysis of overall power utilization

Simulation Temperature (°C)	**Total Power Consumption**	
	Existing NVMSFF (µW)	**Proposed Modified NVMSFF(µW)**

-25	3.376	0.164
0	4.592	0.172
25	5.811	0.177
50	7.046	0.182
75	8.281	0.186
100	9.516	0.190
125	10.772	0.193

Memory circuits with high performance, low power consumption, and small size are now being developed thanks to the improvements made to the proposed improved NVMSFF's circuitry. The power consumption data for the 4x4 and 8x8 memory array architectures developed utilising both the existing NVMSFF and the suggested improved NVMSFF are shown in Table-IV and amply demonstrate this progress. Data clearly shows that memory array structures developed using the proposed terms of performance. Notably, when building higher-order memory array layouts, these variations in power usage become even more obvious. These results highlight the scalability and potential of the modified NVMSFF suggested method to considerably enhance the performance and efficiency of memory circuits, especially as the complexity and size of memory arrays increase.

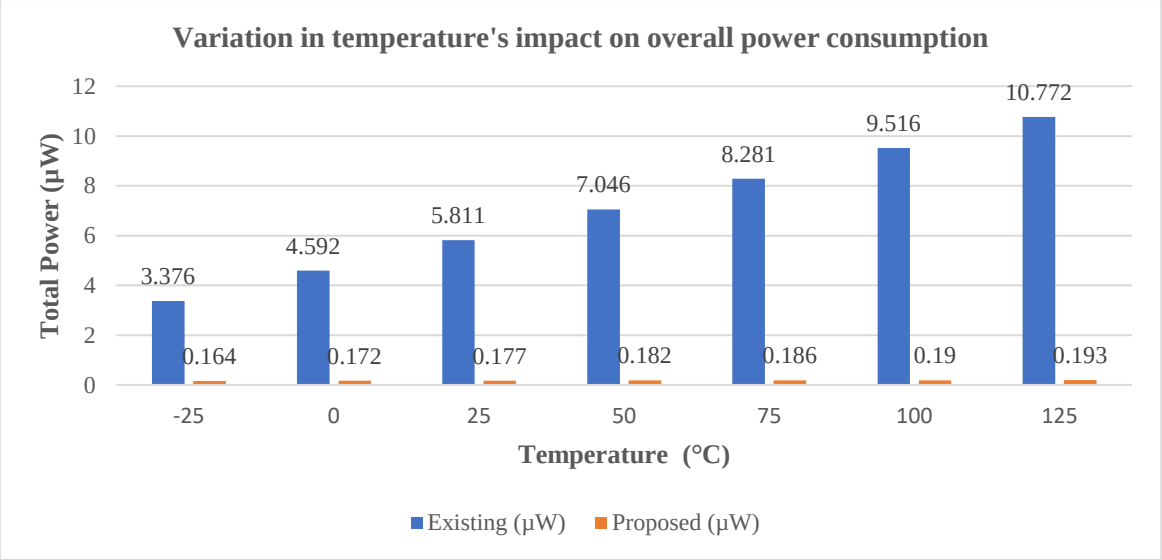

Fig.-12.Changes in temperature's impact on overall power consumption

Table IV. Different-sized memory arrays' overall power use

Size	Methodology	Total Power Consumption (µW)
4x4	Existing NVMSFF	24.93 µW
4x4	Proposed Modified NVMSFF	1.697 µW
8x8	Existing NVMSFF	97.87 µW
8x8	Proposed Modified NVMSFF	4.806 µW

4. Conclusion

The goal of this study is to advance the development of Torque in spin orbit (SOT): controlled devices for magnetic tunnel junctions (MTJs) that energy-efficient, with a focus on improving the speed and energy efficiency of three-terminal PMTJ devices. This study introduces a revolutionary modified circuit that is intended to being low-power, quick, and space-efficient. In comparison to current NVMSFF circuits, this circuit significantly fewer transistor devices. Using the 45nm CMOS process technology and Cadence Virtuoso Tools, the research was completed successfully. The Cadence Spectre tool is part of the ADE for the Cadence Virtuoso Analogue Design Environment. Was used to simulate circuits. Both 4x4 and 8x8 memory arrays were created and compared utilising both the current NVSFF and the newly proposed NVMSFF in order to assess the efficacy of the suggested alterations. The study's findings showed that the modified NVMSFF worked better than the existing NVSFF in terms of fewer delays, less area consumption (it used around 44% less area), and less power usage. Additionally, the suggested NVMSFF-designed memory arrays showed improved energy and space efficiency. The construction of memory chips or higher-order memory array designs appropriate for low-power and fast CPUs is one of the potential applications of this research. Additionally, the suggested modified NVMSFF circuit based on the SOT-PMTJ model shows potential for usage in the construction of finite state machines and other real-time applications. In conclusion, this study emphasises the benefits of combining CMOS and Spintronic technologies to build memory circuits that are more effective, with potential applications in real-time and low-power computers.

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