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Performance of 9T SRAM Cell using Boolean algebra and Arithmetic Operations

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Abstract. This work aims to implement the Boolean and Arithmetic functions with Static Random Access Memory (SRAM) Cell made by nine CMOS Transistor for In-Memory computation. Normally the Von-Neumann architecture is used for current computing system where data and programs are placed in a single memory by sharing and a single Bus is used for memory access, ALU and for controlling of program. This results in minimizing the efficiency of computing when there is high eminence on Data tactless applications. The Von-Neumann architecture is made more efficient by Computation in Memory (CIM) architecture which overcome the drawback of Memory barrier, the power utilization and in the resemblance of wall structure. Here is presented an inside the memory computation method and co-designs of arithmetic circuitry using 9T SRAM cell. The Boolean algebra and Arithmetic operations are illustrated with 9T SRAM cell designed by CMOS technology in 180 nm process. The Boolean algebra for AND- NAND, OR-NOR logic gates are illustrated using 9T SRAM cells with the Latch type sense amplifier to verify the capability of computation in Memory of 9T SRAM cell. To illustrate the arithmetic circuit an array of memory has been made by the 9T SRAM cell and proposed sensing amplifier which is latch type and finally is mapped with circuit of half-adder and half-subtraction.

Index Terms— *CIM- Computation in Memory, 9T- Nine Transistors, SRAM- Static Random Access Memory.*

Introduction

The computing system used now days are based on Conventional von-Neumann architecture. [1]. There are two separate section, one for storage and the other for computation, as shown in Figure 1(A). Due to these separated sections of Memory and section of computation, a large energy is used for data transfer between them. The separation of Memory and computation section results in slow data transfer rate as in this architecture, a processor is remained idle when the Memory is accessed.

A technique used to overcome this drawback is done by Computation in Memory- CIM as shown in Figure 1(B).

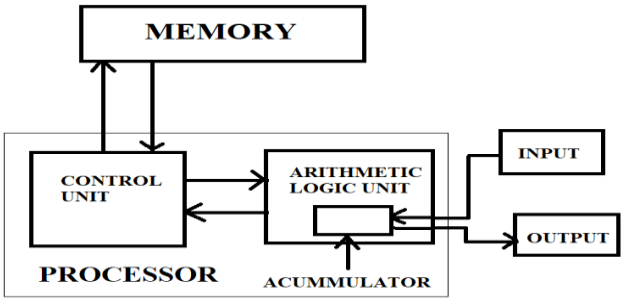

Fig. 1. (A) Computing system architecture as per Von-Neumann

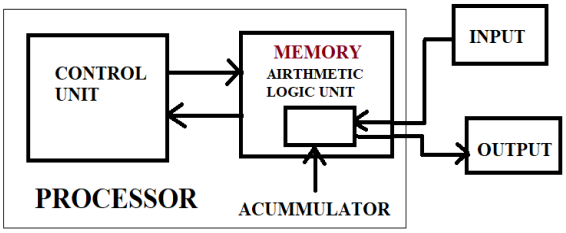

Fig. 1. (B) Computing system architecture as per In-Memory computation.

Here the computation unit is merged with the Memory unit and work as computation done in Memory. And hence the energy is saved and processing speed is made faster than the conventional architecture.

Next is described the Literature review of the previous work done in this topic. And then is the explanation of the structure of the 9T SRAM with its in Memory computation operation.

Next is the Arithmetic function operated in 9T SRAM array of Memory and then the experimental techniques.

In the last is the discussion of measured results for 9T SRAM bit cell and finally conclusion.

Literature Review

The 'In memory based computation' system using SRAM cell made of CMOS shows better performance for the arithmetic and logical operation using 9T SRAM [1] as compared to the operation performed for the 8T SRAM [2]. As examined for large data application von- Neumann bottleneck has greater impact on the speed of computing and utilization of energy for computation [3]. This is overcome by the proposed 9T SRAM bit cell which gives better result in terms of efficiency and noise margin. Non-von Neumann computing architecture is introduced for the computation and storing of the data at the nanometer scale [4]. A configurable content addressable memory is proposed which maintains the density for a push-rule of 6T SRAM cell [7] and is used for storing a 1 bit data. Reading and writing stability of the 6T SRAM is investigated. The hold and standby mode of SRAM for data retention voltage is the minimum voltage by which the state of SRAM is flipped [10]. From all these literature we see the In – memory computation is more robust for large data computation as compared to Von- Neumann computation architecture and also support for storage and operation on bit for the implementation of arithmetic and logical operations efficiently.

Here, is implemented the in-Memory computation for Boolean and Arithmetic operations using bit-cell of 9T SRAM and a sensing amplifier which is latch type, by this method the sense margin is improved for NAND logic gate as represented in Figure 2(A)-(B).

As compared in terms of read noise margin for 9T SRAM cell with 8T SRAM cell and conventional 6T SRAM, 9T SRAM cell makes read operation unique and enables in memory computation.

Read operation is done from transistors T8 and T9. The transistor T7 is used to reduce the write noise margin by which the efficiency of read and write operation increases as represented in Figure 2(A).

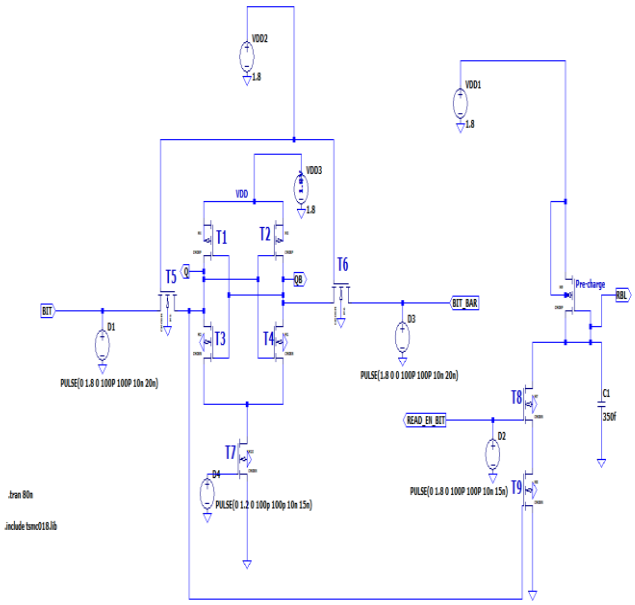

Fig. 2. (A) Circuit diagram of 9T SRAM Cell.

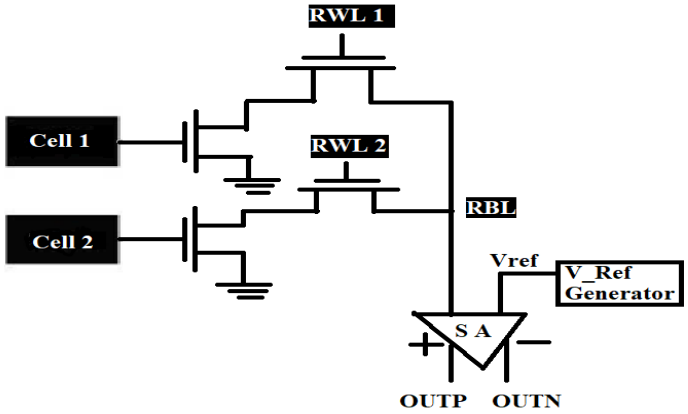

Fig. 2. (B) Schematic of In-Memory Computation With 9T SRAM Cell and a Sense amplifier [3].

In Memory Computation Using 9t Sram

All the three processing operations namely computation, then movement and finally data storage are operated inside the Memory. The basic principle behind 9T SRAM based in memory computation [1] is to enable more than one read word lines concurrently in 9T SRAM array and provides the complete isolation of data from bit lines or the Memory cell. And thus prevents the sneak path and thereby provide more stability of data read and data write operation. This reduces the leakage power compared to 6T, 7T, and 8T SRAM cell.

Write operation of SRAM [7][8], the data is stored into a 4T cell that is T1, T2, T3,T4 CMOS which are in back to back configuration.

Read operation is done from transistors T8 and T9. The transistor T7 is used to reduce the write noise margin by which the efficiency of read and write operation increases as shown in Figure 2(A).

Implementation Of Boolean Function

The realization of the Boolean logic gates operation for two input operands, two SRAM cells are used, the output of which is taken through a sense amplifier. The sense amplifier works as to sense the change of RBL voltage which arises due to the two operands. Here is used a sensing amplifier which is latch type [9] with 350F Read Bit Line capacitor value for in memory computation operation through 9T SRAM. For this purpose to read word line are enabled simultaneously and the voltage VRBL and reference voltage V_Ref = 1.2 Volt is connected to sense amplifier. As shown in Figure 2(B). Initially VRBL is pre-charged to VDD. This pre-charged VRBL will either the discharged or will beat pre-charged state as per the value of stored bit in the Memory cell.

A. REALIZATION OF NOR/OR BIT-WISE WORKING

The performance of NOR/OR gates are realized through 9T SRAM cell by using sensing method as given in Figure 3(A).

Here the terminal which is positive is connected to the VRBL and the terminal which is negative is connected to the VREF-NOR. For VREF-NOR, the value is taken between VRBL at values "01/10" and VRBL at value "11". Hence through VRBL different values of bit is stored into a cell. For only the value of VRBL "00" that is when both bits are '0', sense amplifier output will be at logic '0' for the terminal which is positive and output of logic '1' for the terminal which is negative.

OR operation is represented by the positive terminal and NOR operation is represented by the negative terminal at the sense amplifier when the sense enable pin is high.

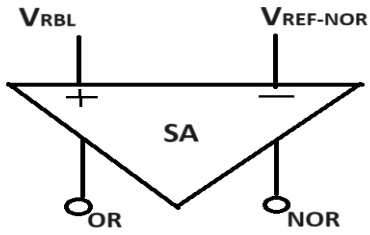

Fig. 3. (A) Sense method for OR and NOR logic.

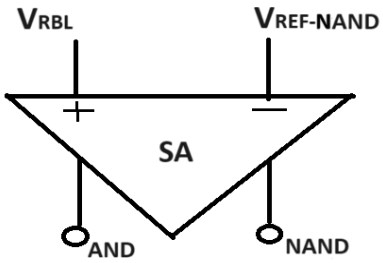

Fig. 3. (B) Sense method for AND and NAND logic.

B. REALIZATION OF NAND/AND BIT-WISE WORKING

The working of NAND/AND logics are realized through 9T SRAM cell by using sensing method as given in Figure 3(B), Here the positive terminal is connected to the VRBL and negative terminal is connected to the VRef-NAND. For VRef-NAND, the value is taken between VRBL at values “01/10” and VRBL at value “00”. Hence through VRBL different values of bit is stored into a cell. For only the value of VRBL “11” that is when both bits are ‘1’, sense amplifier output will be at logic ‘high (1)’ at the terminal which is positive and output of logic ‘low (0)’ at the terminal which is negative.

In the same manner as OR/NOR logic the AND operation is represented by the positive terminal and NAND operation is represented by the negative terminal at the sense amplifier when the sense enable pin is high.

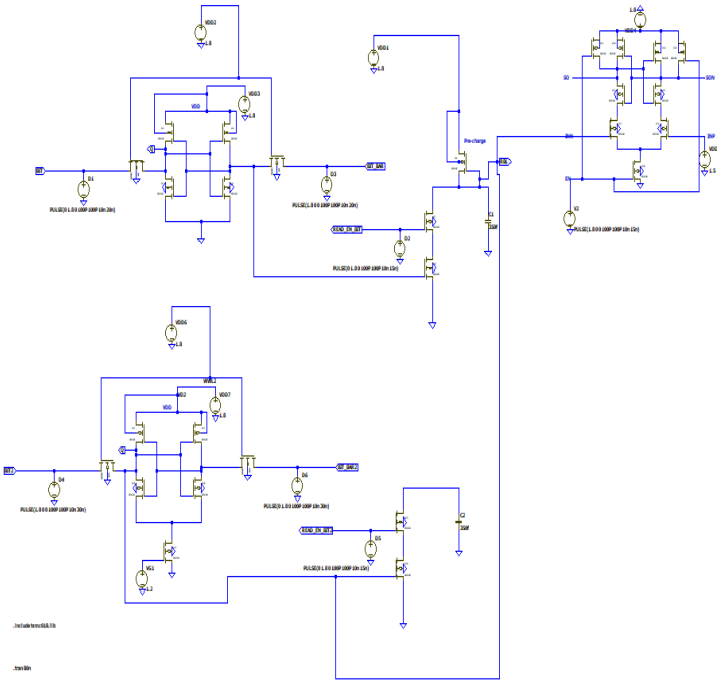

Fig. 4 (A) Logical Implementation by In-Memory Computation.

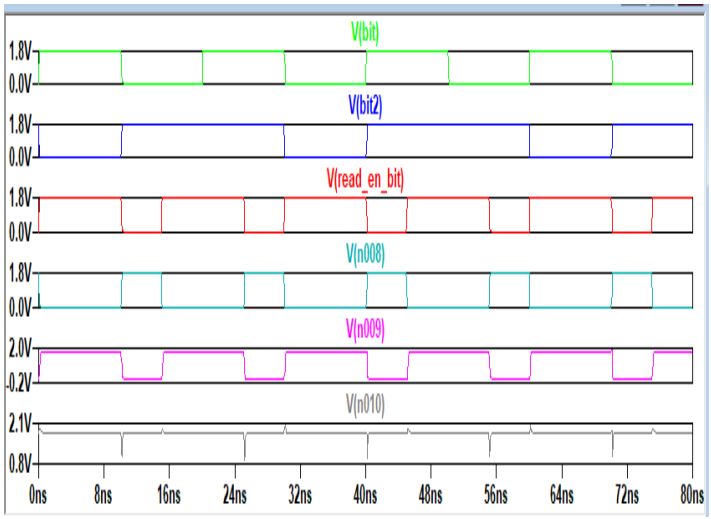

Fig. 4. (B) Simulation result of logical implementation.

Arithmetic Operation

The array of 9T SRAM cell comprises of SRAM bit cell, a circuit for pre-charge and a circuit for sense operation. The NMOS transistor is used for pre-charge circuit and sense amplifier circuit is latched type.

The NOR logic is serially mapped to get the

functionality of Half Adder circuit as shown in the figure. And hence Half Adder is implemented using 9T Static RAM bit cell and the scheme for sense operation.

C. HALF-ADDER OPERATION

Implementation of Half -Adder is done by the Memory array of 2 X 5 size as shown in the figure 5(A).It comprise of five NOR gates and two one bit binary numbers namely A and B. From here we get the two outputs of 1 bit numbers for a SUM representation and to represent a CARRY respectively.

SUM = A $\oplus$ B

CARRY = A * B

This operation requires one number of column and two numbers of rows of 9T SRAM array forming the 2 X 5 SRAM and mapped serially with five NOR net list.

First the two operands A and B are stored in the SRAM bit cell. Then the RBL is pre-charged to VDD by the pre-charge circuit. Across each NOR gates some delay is arrived. The circuit is properly pre-charged to get the correct result. Due to delay of each NOR gate, the RBL of nearest column is pre-charged when the input is occurred from the previous NOR column and finally we simulate the NOR logic gates mapped with the SRAM array to get the output for Half Adder for every combinations of input.

Representation of array of Memory as shown:

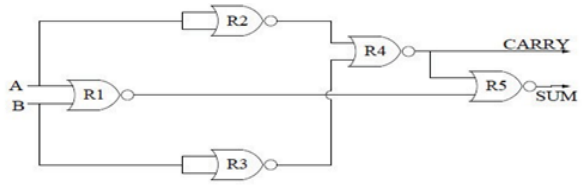

Fig. 5. (A) Circuit Diagram of Half adder using NOR net-list.

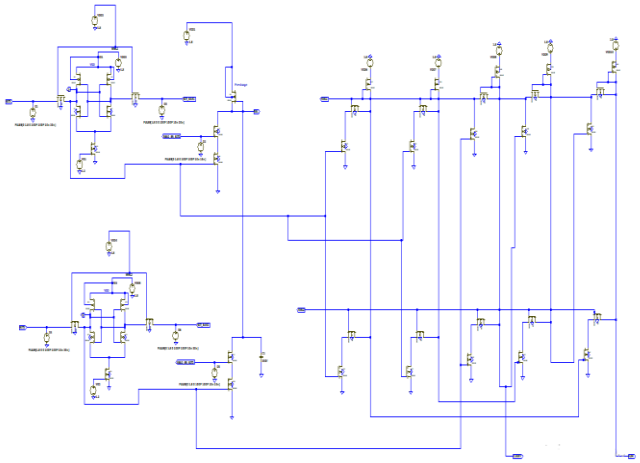

Fig. 5. (B) Arithmetical Implementation of Half Adder by In-Memory Computation

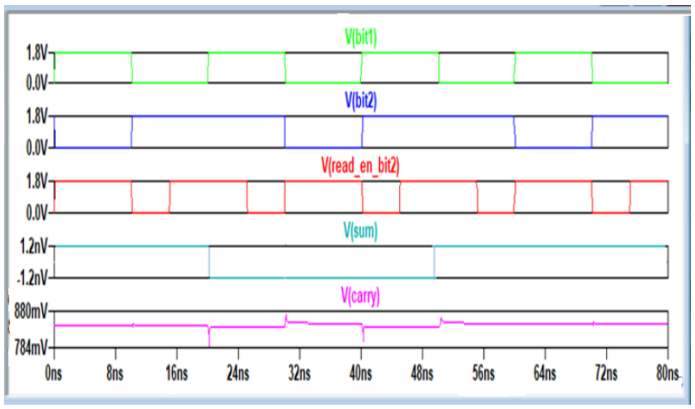

Fig. 5. (C) Simulation result of Arithmetical Implementation of Half Add

D. *HALF SUBTRACTOR*

Implementation of Half Subtraction is done by the Memory array of 2 X 5 size as shown in the Figure 6(A).It comprise of five NOR gates and two one bit binary numbers namely A and B. From here we get the two outputs of 1 bit number for a 'DIFFERENCE' and a 'BORROW' respectively.

'DIFFERENCE' = A ⊕ B

'BORROW' = A' * B

This operation requires 1-column and 2- rows of 9T SRAM array forming the 2 X 5 SRAM and mapped serially with five NOR net-list.

First the two operands A and B are stored in the SRAM bit cell. Then the RBL is pre-charged to VDD by the pre-charge circuit. Across each NOR gates some delay is arrived. The circuit is properly pre-charged to get the correct result. Due to delay of each NOR gate, the RBL of nearest column is pre-charged as when there is an input due to the previous NOR-column and finally the NOR logic gate is simulated which is mapped with the SRAM array to get the output for Half Subtraction for every combinations of input.

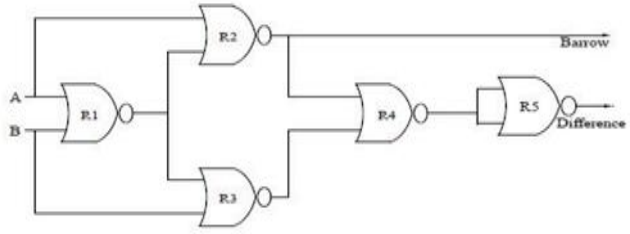

Fig. 6. (A) Circuit Diagram of Half Subtraction using NOR net-list.

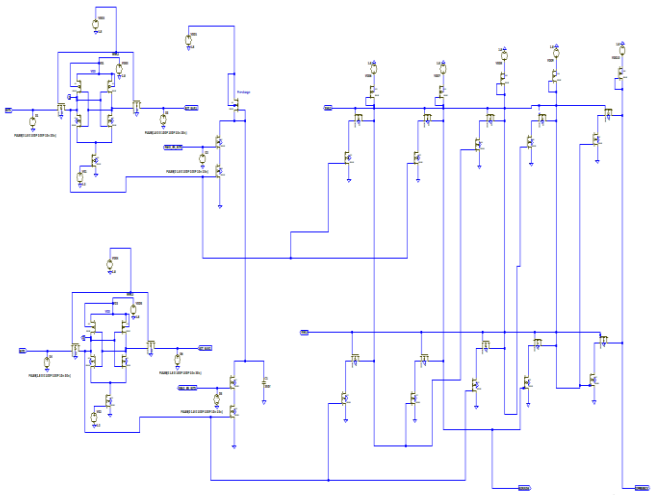

Fig. 6. (B) Arithmetical Implementation of Half Subtractor by In-Memory Computation

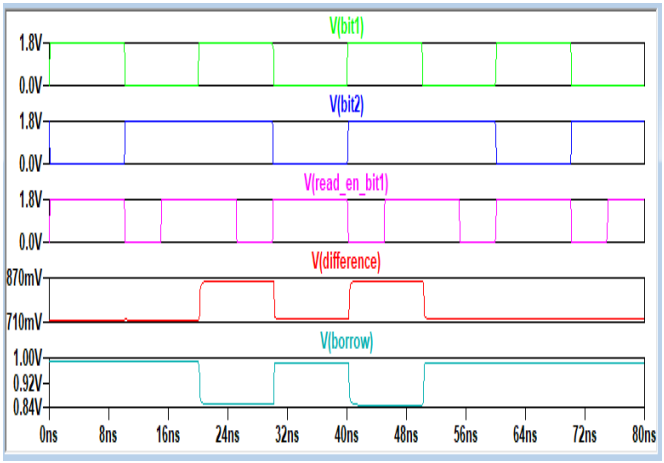

Fig. 6. (C) Simulation result of Arithmetical Implementation of Half Subtractor

Results And Discussion

Here the average power consumed in the In Memory computation for Boolean logic operation and Arithmetical operation with corresponding energy consumption for 6T, 7T 8T and 9T SRAM as shown in the following Table. We observe the results obtained for different SRAM and when compared the 9T SRAM shows better performance in terms of average power and energy for different operations.

I. Average power and Energy analysis for 6T SRAM

6T SRAM Operation	Average Power in µW	Energy in fJ
Write Operation	20.36	162.9
Read Operation	6.6521	532.1
AND Operation	256.41	0.021
OR Operation	31.644	2.531
Sum Operation	92.389	739.1
Carry Operation	89	712.0

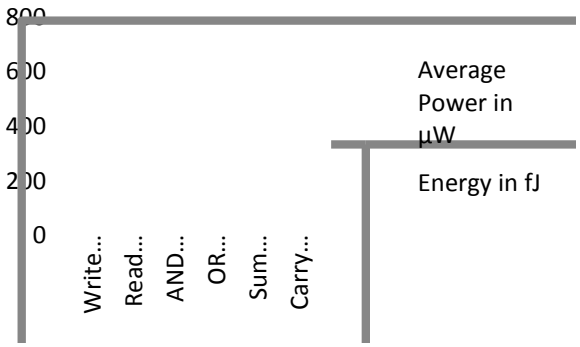

Fig. 7. Representation of 6T SRAM operation

We observe the results obtained for conventional 6T SRAM which is designed for low noise margin [14] [15] [17] [19] and the performance is analyzed for logical and arithmetical operations.

II. Average power and Energy analysis for 7T SRAM

7T SRAM Operation	Average Power in µW	Energy in fJ
Write Operation	208.34	16.67
Read Operation	184.51	0.147
AND Operation	172.67	1.381
OR Operation	348.93	2.791
Sum Operation	193.64	15.49
Carry Operation	86.095	0.0068

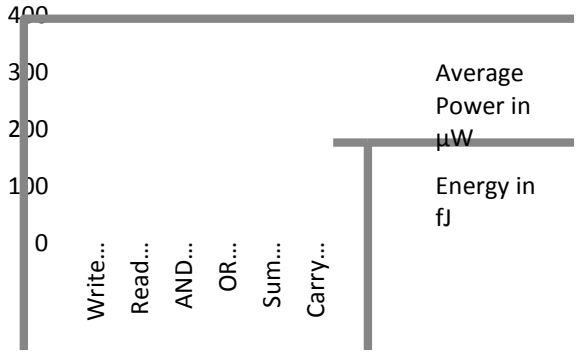

Fig. 8. Representation of 7T SRAM operation

We observe the results obtained for the 7T SRAM which is designed for robust and low power consumption [17] [19] and the performance is analyzed for logical and arithmetical operations.

III. Average power and Energy analysis for 8T SRAM

8T SRAM Operation	Average Power in µW	Energy in fJ
Write Operation	16.241	129.9
Read Operation	5.7262	458.1
AND Operation	69.59	55.678
OR Operation	25.30	20.24
Sum Operation	46.16	369.2
Carry Operation	88.05	704.4

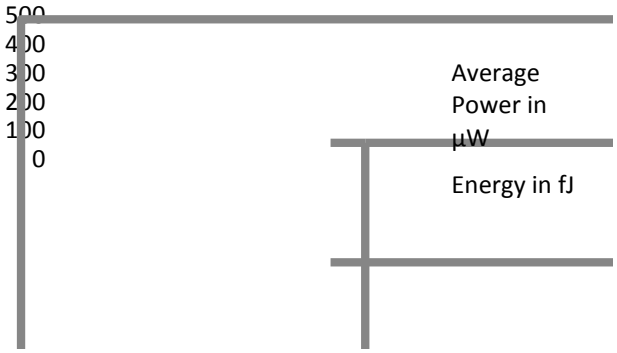

Fig.9. Representation of 8T SRAM operation

Again we observe the results obtained for the 8T SRAM with a higher read noise margin [2] [20] and the performance is analyzed for logical and arithmetical operations with CMOS technology in 180 nm process.

IV. Average power and Energy analysis for 9T SRAM

9T SRAM Operation	Average Power in µW	Energy in fJ
Write Operation	63.14	5.051
Read Operation	0.401	32.06
AND Operation	0.053	4.227
OR Operation	0.218	17.43
Sum Operation	138.11	11.05
Carry Operation	43.76	350.13

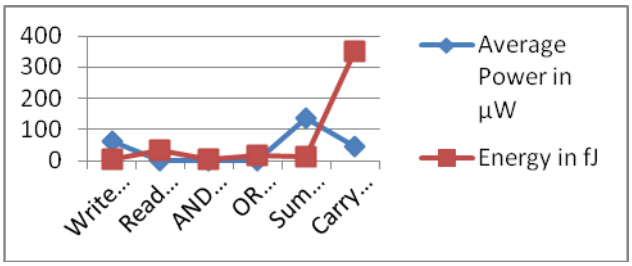

Fig. 10. Representation of 9T SRAM operation

All the results obtained are compared with the performance of 9T SRAM cell for different operation. Here we observe that the average power consumption and energy is less compared with other SRAM cell.

conclusion

The In memory computation with 9T SRAM is shown for analysis of Boolean logic and Arithmetic operation in this paper and is compared with 6T, 7T and 8T. We get the simulation result in LT Spice with CMOS technology in 180 nm process for various operations and the performance of every operation is found to be good when compared with other technology. It shows better energy efficiency for all operation and less power consumption.

The 9T SRAM has higher energy efficiency for different operations and also perform well in logical and arithmetical operation which represents the feasibility of computation in the array of SRAM cell. A great approach is available for fast computing using 9T SRAM Cell for any type of computation.

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