Tuijin Jishu/Journal of Propulsion Technology
ISSN: 1001-4055
Vol. 44 No. 3 (2023)

21 Level Asymmetric Inverter without Inversion Circuit with Reduced Switch Count for BLDC Motor Drive

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Abstract - Design for asymmetrical Multi-Level Inverter without H-bridge and with minimal number of switch is presented in this paper. The proposed circuit is capable of generating 21 levels with only 10 switches and 3 unequal D.C.voltage sources. Operation of the proposed circuit is discussed in detail in this paper and there by framing the switching sequence for the proposed circuit. Simulation of the presented inverter is done for loads like resistive, reactive and induction motor. From the simulation results, inverter performance is analyzed in terms of THD.
Keywords - Asymmetric inverter, modes of operation, multi-level inverter, power electronics, reduced switch component.

1. Introduction

Multi-Level Inverters (MLI) have become a revolutionin the world of power electronics for its improved voltage and current waveforms, high power applications and for power quality demanding applications. They also find applications in speed drive control, STATCOMS, HVDC and HVACtransmissions. The advantages of multi-level inverters are used in higher voltage operability, reduced voltage derivatives, reduced voltage harmonic components, fault tolerant operation and increased efficiency. The current trend applications for multi-level inverters are around photovoltaic conversions, electric vehicle technology, wind energy technology etc. Multi- level inverter consists of various circuit components such as diodes, voltage sources and switches. Based on theconstruction of the circuit and the voltage sources considered, the inverters are classified assymmetric and asymmetric MLIs and to be specific they are further classified as cascaded H-Bridge, diode clamped and flyingcapacitor inverters [1]-[2].

In symmetric MLIs, the D.C. sources have the same amplitude in their configuration, whereas in asymmetrical inverters the sources have non identical source ratings in their configuration. All these types of conventional type MLIs havea greater number of switches in their design which directed toconstruct MLI with reduced components. As reduced numberof switches is required, asymmetrical MLIs are identified foroperation. Due to the reduced switch count, the switching power losses are lowered drastically.

Also, another big advantage of asymmetrical configuration is that for the same switch count, higher level can be obtained in asymmetrical configuration compared to symmetrical configuration. Required parameters for the design of a MLI are number of levels to be acquired, count of the switches needed for the required levels, harmonic occupancy in voltage obtained at output, the count of independent D.C. sources needed to generate the required +levels, switch stress and the standing voltage.

However, for achieving higher unit steps, more oflevels, a greater quantity of switches are required. So,a solution is needed to have additional levels and to have reduced switching components [3]-[6]. For better performance of the MLI, the harmonic distortion finds a crucial role. The achievement of theMLI can be inferred from the amount of harmonic distortion present at the loadcurrent and voltage. Theharmonic distortion must be reduced so that the MLI performance can be improved. Forthe reduction of harmonic distortion, the PWM techniquesengaged in the semiconductor switches plays a central role.This also helps in providing the required switching patternsuch that we get a sinusoidal wave across the load.

Considering the above, many attempts are being made in the past few years to reduce the switch count and those works are discussed in [7]-[11]. These works have given some new structures and topologies with reduced count but having its own shortcomings. The proposed model is also a new topology structure with reduced switching component and taken into consideration of the shortcomings to produce a much higher level of output. The proposed model is a new topology for 21-level asymmetric MLI with only 10 switches and 3 unequal D.C. sources. The configuration does not possess inversion circuit, there by operability of the circuit is increased for higher range of voltages.

This paper follows through as given in section II describes the model of proposed circuit, the analysis of switch count, level count and the peak voltage followed by section III which provides the working, modes of operation and the switching sequence of the proposed circuit in a detail manner. Section IV is the results of the proposed model from the simulation. Finally in Section V, conclusions are made on the proposed model which gives a higher voltage with reduced switch count and reduced THD.

2. 21-Level Inverter With Switching Sequence

A MLI configuration without inversion circuit is shown in figure 1. To obtain 21 levels, the proposed circuit consists of 10 switches and 3 voltage sources. Here, all 10 switches are uni-directional in nature as illustrated in figure 2, so that identical driver circuit is used for the switches present in the circuit. A basic sinusoidal PWM technique is used generating triggering pulses for the proposed model. The designed MLI circuit is formed with 3 unequal voltage sources which will make an asymmetric configuration. D.C. voltage sources are identified as 40V, 80V and 280V respectively.

A. MLI Design Criteria

For the inverter topology, mathematical equation is derived with the aim of finding the level count obtained from the inverter and switch count and the voltage sources required for the inverter. Let the voltage sources required be switch count be N_{SW}, level count of the inverter be N_{lvl}.

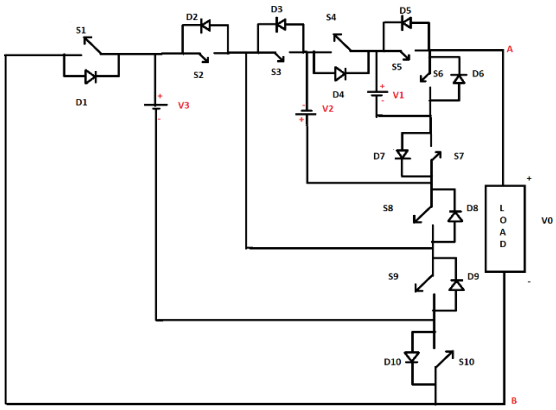

Fig 1: 21 Level Inverter [12]

Fig 2: Switch Configuration

The switch count for the proposed inverter can becalculated as given in Equation 1,

Nsw = 2m + 2---------- (1)

The level count for the figure 1 can be calculated fromEquation2,

Nlvl = 7 × m ----------(2)

The peak output voltage of the inverter is achieved from Equation 3,

V0, max = (2m + 2) × VDC ----------(3)

Now the proposed topology consists of 3 voltage sources ($m = 3$), so switch count N_{SW}= 10, the level count of the inverter is $N_{lvl} = 21$. Here the VDC = V1 = 40V, so thepeak output voltage can be given as V0, max = 400V.

B. Pulse Generation

The pulses that are to be given to the switches are generated by using four divisions, sine wave signal asreference, comparator for comparing the reference wave and the gain, relational and logic circuit are used for producing the pulses for the switches and driver circuits forthe triggering of the switches. These four divisions canbe demonstrated as illustrated in figure 3.

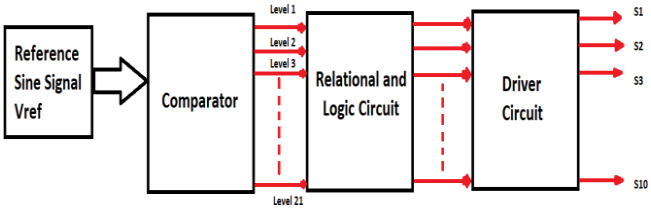

Fig 3: Various Divisions of Pulse Generation

From the block diagram (Figure 3), a sine wave is takenas reference and the amplitude of the reference wave is taken as 11V. Its chosen based on the positive level and zero level needed for the MLI. This reference wave is given as the input to the comparator. The output of the comparator obtained is directed to relational and logiccircuit block. Here relational operators are used to comparethe levels that are to be selected. For each level a pair of relational operators and an AND gate is used for the generation of the pulses. This output is sent to a driver circuit which consists of a sum block and multiport switch block. The sum block collects all the pulses that is to be selected for each switching sequence. The multiport block is used to provide the switching sequence in which the switches are to be turned on. For each level the multiport block is coded with switching sequence of the respective level as its input. Now all the four divisions areimplemented for each level coded with their respective switching sequence and then given to the IGBT switches used in the proposed configuration.

3. Modes Of Operation

The inverter is designed to work in 21 modes of operation to construct an alternating waveform. For understanding purpose; few modes are explained in figure 3 Device status for each mode of operation is given below,

Mode-1:S2, S3, S5, S7, S10 devices are ‘ON’ to generate400V
Mode-2: S2, S3, S6, S7, S10 devices are ‘ON’ to generate360V
Mode-3: S2, S5, S7, S8, S10 devices are ‘ON’ to generate320V
Mode-4: S2, S3, S4, S5, S10 devices are ‘ON’ to generate280V
Mode-5:S2, S3, S4, S6, S10 devices are ‘ON’ to generate240V
Mode-6:S1, S3, S6, S7, S9 devices are ‘ON’ to generate 200V
Mode-7:S2, S4, S6, S8, S10 devices are ‘ON’ to generate160V
Mode-8:S3, S5, S7, S9, S10 devices are ‘ON’ to generate120V
Mode-9:S9, S6, S7, S9, S10 devices are ‘ON’ to generate 80V
Mode-10:S5, S7, S8, S9, S10 devices are ‘ON’ to generate40V
Mode-11:S6, S7, S8, S9, S10 devices are ‘ON’ to generate 0V
Mode-12:S3, S4, S6, S9, S10 devices are ‘ON’ to generate -40V
Mode-13:S4, S5, S8, S9, S10 devices are ‘ON’ to generate -80V
Mode-14:S4, S6, S8, S9, S10 devices are ‘ON’ to generate -120V
Mode-15:S1, S3, S5, S7, S9 devices are ‘ON’ to generate -160V

Mode-16:S_1, S_3, S_6, S_7, S_9 devices are 'ON' to generate -200V
Mode-17:S_1, S_5, S_7, S_8, S_9 devices are 'ON' to generate -240V
Mode-18:S_1, S_6, S_7, S_8, S_9 devices are 'ON' to generate -280V
Mode-19:S_1, S_3, S_4, S_6, S_9 devices are 'ON' to generate -320V
Mode-20:S_1, S_4, S_5, S_8, S_9 devices are 'ON' to generate -360V
Mode-21:S_1, S_4, S_6, S_8, S_9 devices are 'ON' to generate -400V

From the modes of operation, the Table 1 is arrived to show the switching sequence for the different levels of theinverter.

Table 1: Sequence for the switches

Mode	Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o
1	10	0	1	1	0	1	0	1	0	0	1	+400V
2	9	0	1	1	0	0	1	1	0	0	1	+360V
3	8	0	1	0	0	1	0	1	1	0	1	+320V
4	7	0	1	1	1	1	0	0	0	0	1	+280V
5	6	0	1	1	1	0	1	0	0	0	1	+240V
6	5	1	0	1	0	0	1	1	0	1	0	+200V
7	4	0	1	0	1	0	1	0	1	0	1	+160V
8	3	0	0	1	0	1	0	1	0	1	1	+120V
9	2	0	0	1	0	0	1	1	0	1	1	+80V
10	1	0	0	0	0	1	0	1	1	1	1	+40V
11	0	0	0	0	0	0	1	1	1	1	1	0V
12	-1	0	0	1	1	0	1	0	0	1	1	-40V
13	-2	0	0	0	1	1	0	0	1	1	1	-80V
14	-3	0	0	0	1	0	1	0	1	1	1	-120V
15	-4	1	0	1	0	1	0	1	0	1	0	-160V
16	-5	1	0	1	0	0	1	1	0	1	0	-200V
17	-6	1	0	0	0	1	0	1	1	1	0	-240V
18	-7	1	0	0	0	0	1	1	1	1	0	-280V
19	-8	1	0	1	1	0	1	0	0	1	0	-320V
20	-9	1	0	0	1	1	0	0	1	1	0	-360V
21	-10	1	0	0	1	0	1	0	1	1	0	-400V

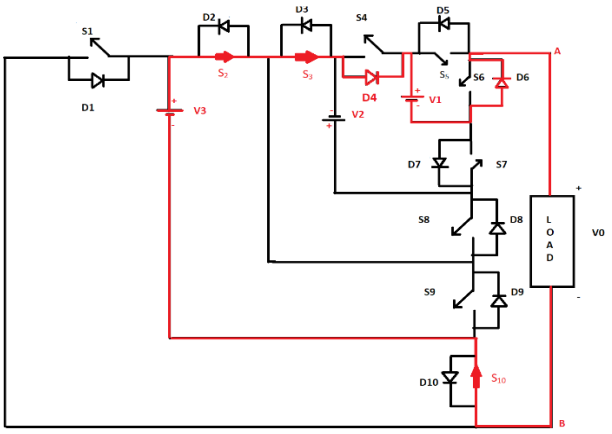

Fig 4 (a): Mode-1 (+400V)

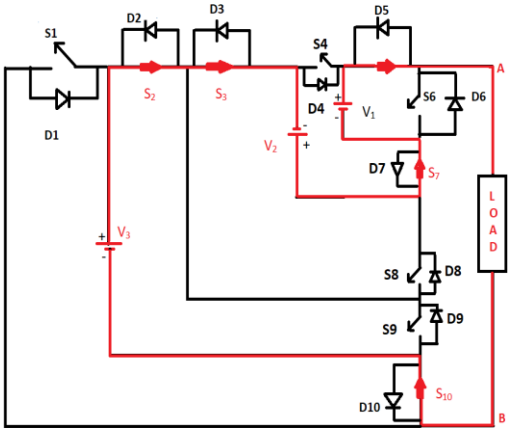

Fig 4(b): Mode-5 (+240V)

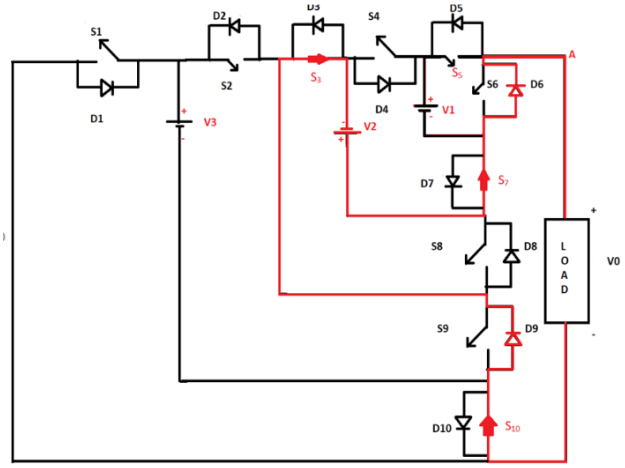

Fig 4(c): Mode-9 (+80V)

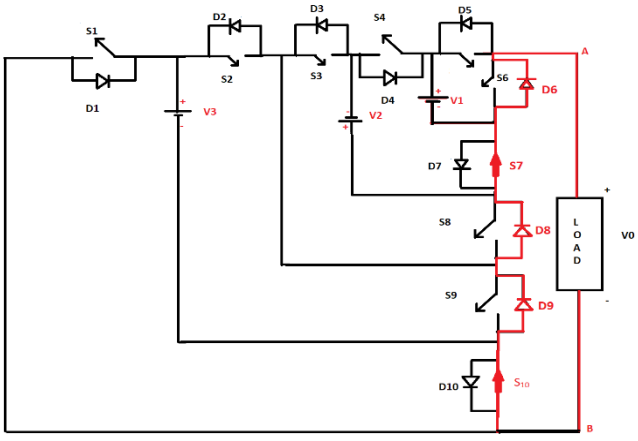

Fig 4(d): Mode-11 (0V)

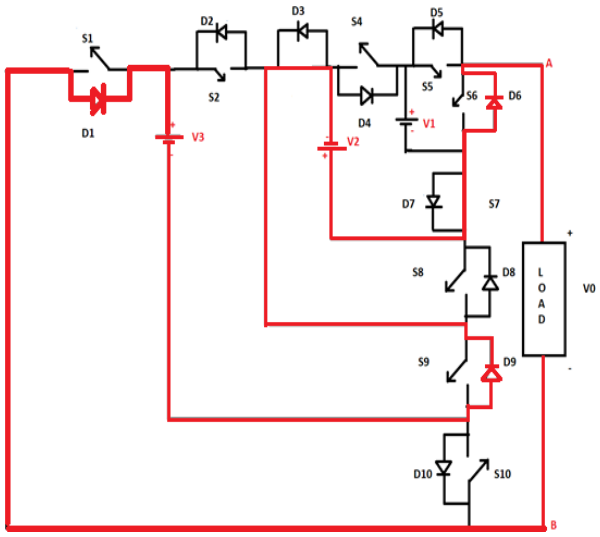

Fig 4(e): Mode-16 (-200V)

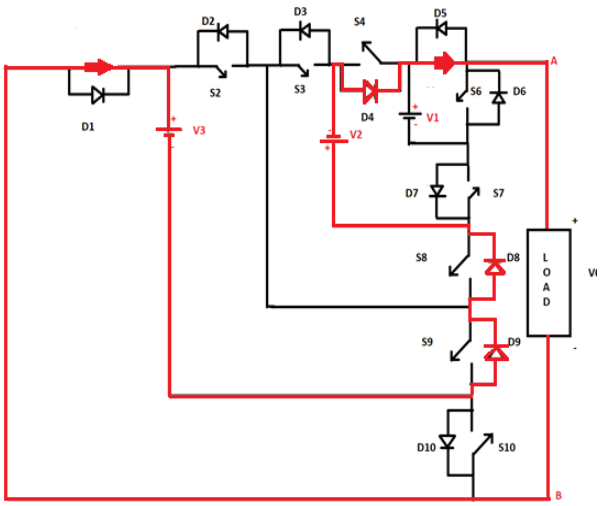

Fig 4 (f): Mode-20 (-360V)
Fig 4: Modes of Operation for 21 level inverters

4. Simulation And Results

In figure 4, the simulated result of the proposed inverter simulated in MATLAB/SIMULINK with resistive load of150Ω is shown. THD of the inverter's voltage wave shapeis 4.73% and it is inside the scope of guidelines given in IEEE 519. The proposed circuit constructs a crest-to-crest voltage of ±400V as illustrated in figure 4.

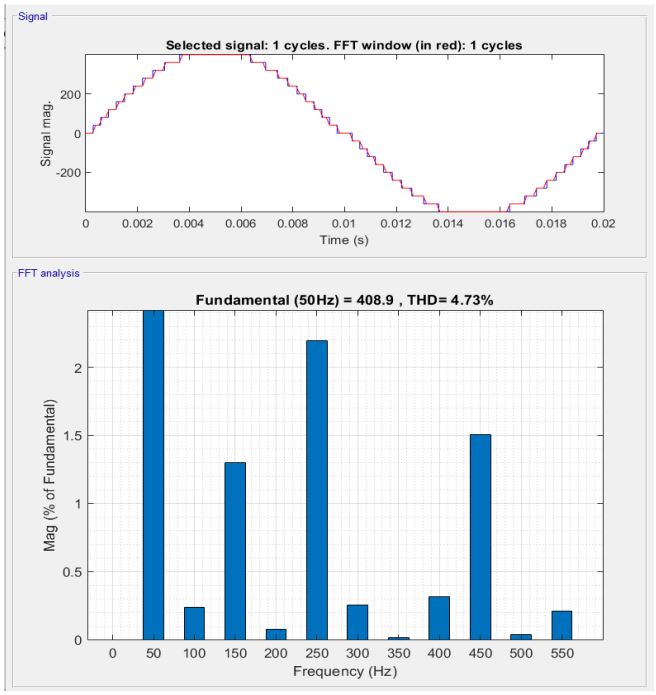

Fig 5 (a): Simulation result of 21-level inverter forRload

Further,the proposed circuit is simulated for a R-L load, with R=150Ω, L = 0.477H. The output voltage for the RL load for the proposed inverter is displayed in figure 5 and the THD for the presneted inverter's output voltage is4.82%.

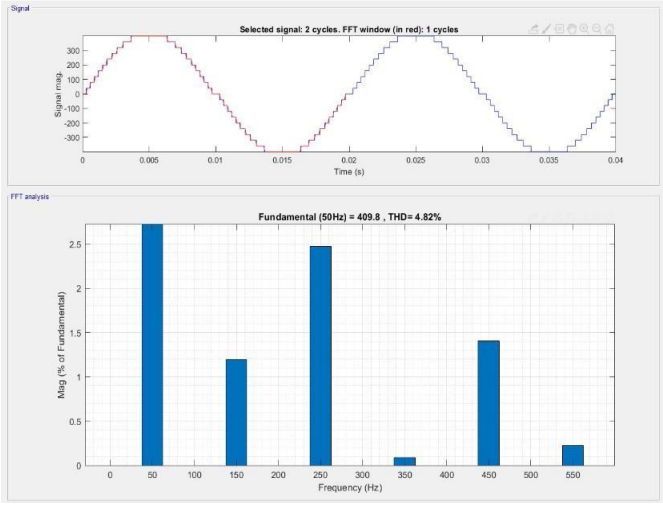

Fig 5(b): Results of the circuit tied with RL Load of 21-level inverter (Voltage THD)

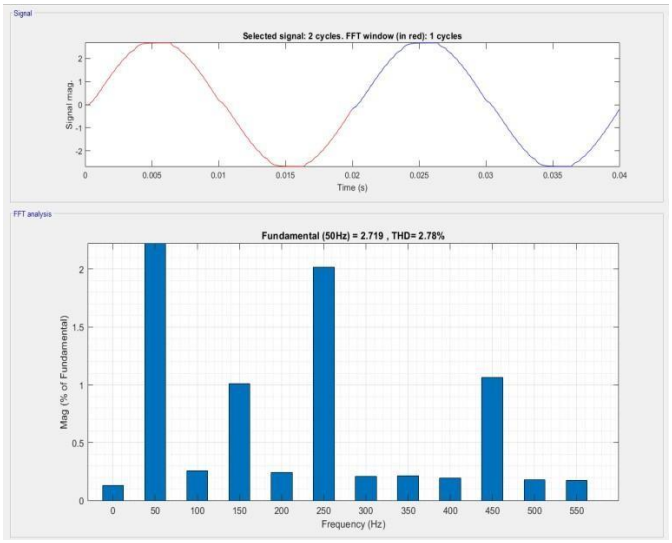

Fig 5(c). Results of the circuit tied with RL Load of 21-level inverter (Current THD)

The proposed circuit is also simulated for inductionmotor load as given in the below figure,

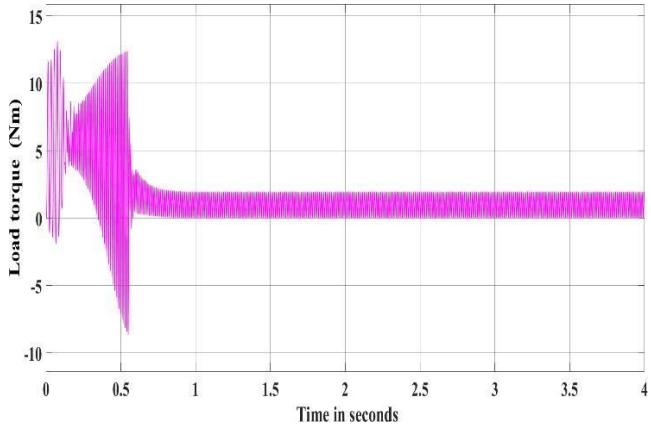

Fig 5(d). Results of the circuit tied with inductionmotor Load of 21-level inverter (main winding current)

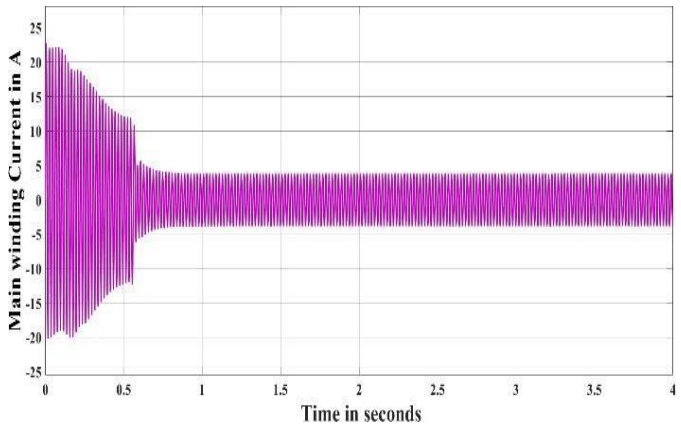

Fig 5(e). Results of the circuit tied with inductionmotor Load of 21-level inverter (Speed)

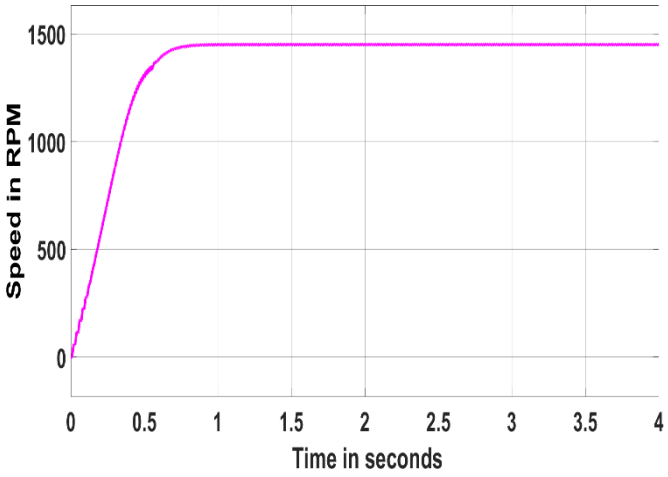

Fig 5(f). Results of the circuit tied with inductionmotor Load of 21-level inverter (Load torque)

When the circuit is tied with an induction motor, the motor settles at a speed of 1451 rpm, due to a load torque of 2 Nm, as presented in figures 5e and 5f respectively. Now the THD of the circuit after connecting it with a motorload is 4.12% that can be shown as,

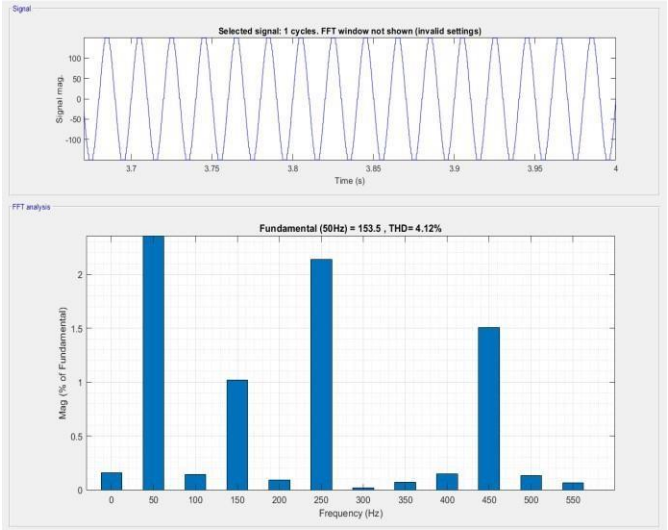

Fig 5(g). Results of the circuit tied with inductionmotor Load of 21-level inverter (Voltage THD)

5. Comparative Study

Multiple structures for the MLI have been presented to reduce the switch count. The structure realized in [13] is a 51-level symmetric structure consisting of 9 level structures in cascade with an H-bridge circuit. This structure has 25 independent sources, each having a magnitude of 1 volt, along with 46 power switches. Due tothe symmetrical structure, achieved output voltage is less, but the circuit has a low THD value of 1.95%. The proposed MLI in [14] 31-levels are obtained using asymmetric configuration. This configuration consists of ten power switches and six independent sources. The negative levels obtained using an H-bridge and the THD value obtained for reactive load is 3.18%. By using the basic principle of CHB inverters, a new cascaded topology is realized in [15]. The basic unit is made of 3 independent sources and 5 power switches. This basic unitis cascaded with H-bridge to obtain multiple levels. Using one base unit 9 levels are achieved with a THD value of 18.8%. Cascading two basic units we obtain 15 levelswith a THD value of 14.16%. By cascading the basic unit,we get the respective levels as 27, 33, 39 and their respective THD values are 12.07, 11.85 and 11.33%. In [16] 57-level inverter is realized having 9 cascaded structures with an H-bridge. The basic unit

consists of 3 independent sources and 6 power switches. The symmetric configuration consists of a total switch count of 51 and 28 independent sources to obtain the 57-level output. Also, the same levels of output can be obtained in an asymmetrical configuration with only two basic units where the switch count is 18 and the number ofindependent sources is seven. Comparative plot on switch count, independent source and THD% for the reference paper [13]– [16] with respective to propose topology is shown in figure 6(a), figure 6(b) and figure 6(c) respectively.

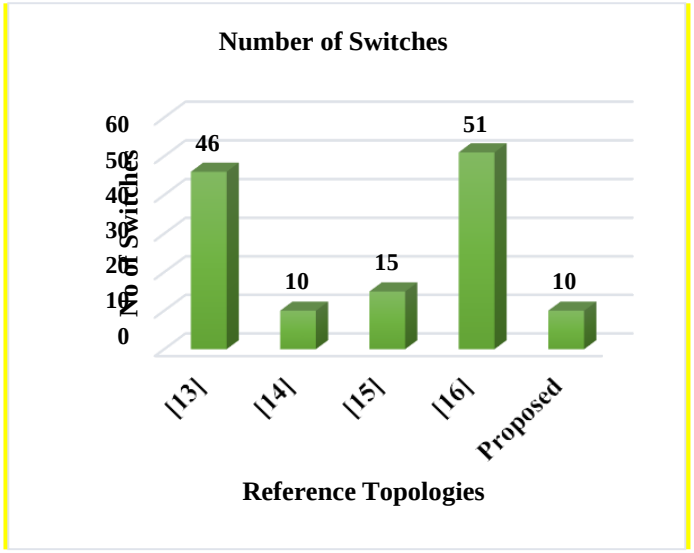

Fig 6(a). Comparative study for switch count

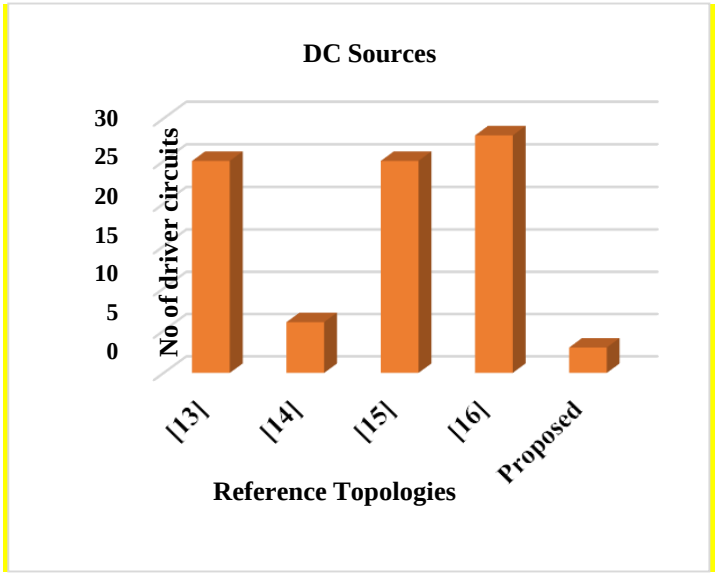

Fig 6(b). Comparative study for independentsources

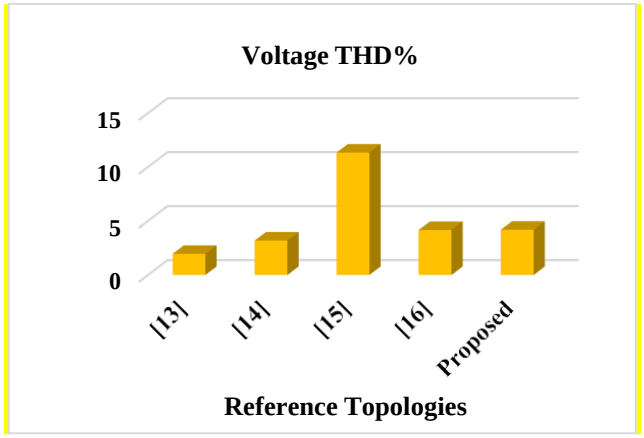

Fig 6(c). Comparative study for THD%

6. Conclusion

A 21-levelconfiguration of MLI which make use of minimal switch count has been discussed in detail in this paper. The proposed circuit can achieve the maximumvoltage with minimum number of switches with a low THD, thereby reducing the cost and size. Comparison between the proposed circuit with traditional inverters such as cascaded H-Bridge, diode clamped and flying capacitor invertersare demonstrated from figure 7 (a) to figure 7 (e).

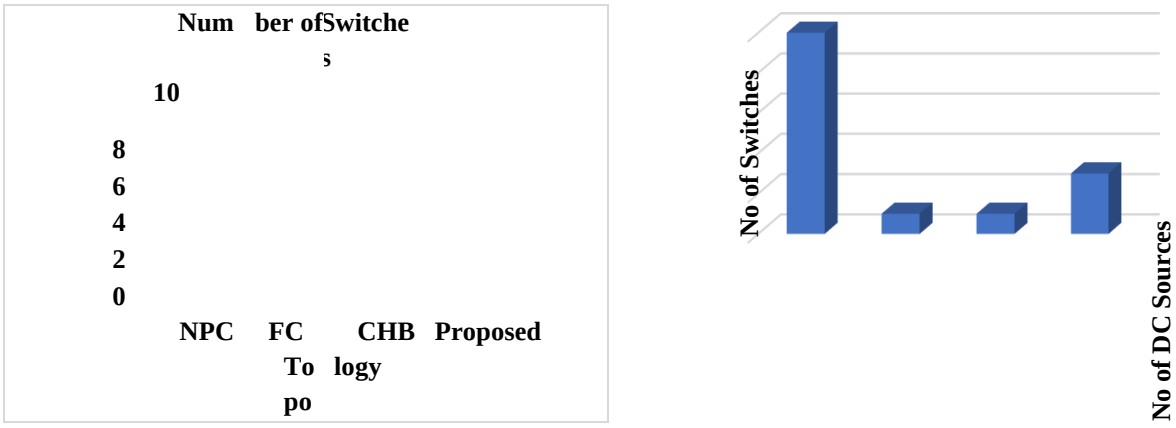

Fig 7(a). Number of Switches

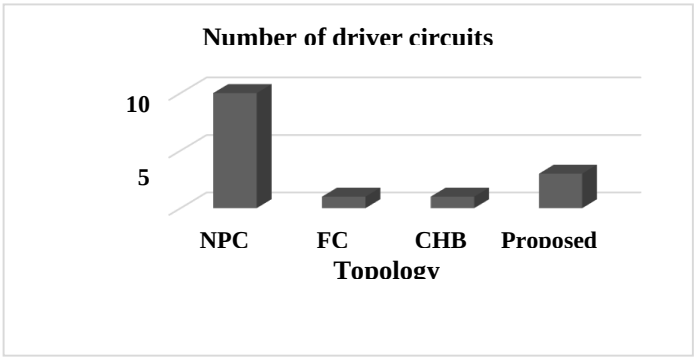

Fig 7(b). Number of driver circuits

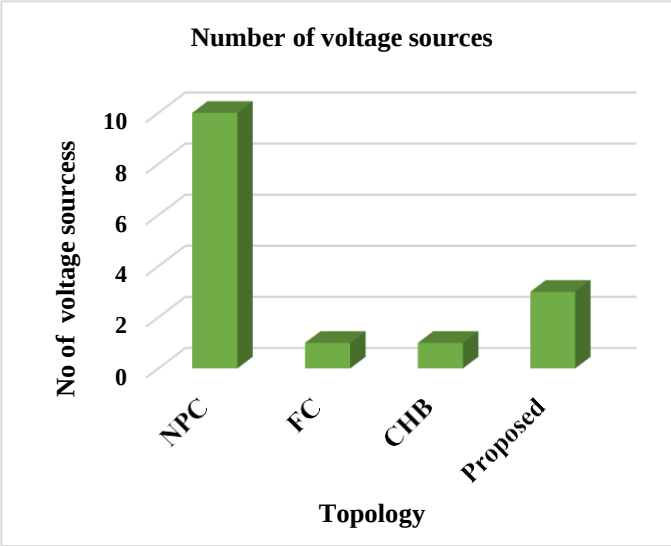

Fig 7(c). Number of voltage sources

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