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Automated Visual Inspection in the Era of Pervasive AI: A Systematic Review of PCB Defect Detection Methodologies (2020– 2026)

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Abstract:- As the global electronics industry transitions toward the Industry 4.0 framework, the miniaturization of Printed Circuit Board (PCB) components has outpaced the capabilities of manual inspection, necessitating a shift toward Pervasive Automated Visual Inspection (AVI) systems. This systematic review rigorously analyzes 40 seminal research works, documenting a critical architectural metamorphosis from traditional referential image processing to advanced global-context architectures. We categorize these methodologies into a multi-tiered taxonomy, evaluating the evolution of one-stage detectors from YOLOv5 to the high-resolution, deformable-convolution-enabled YOLO11. A focal point is the transition toward the new frontier of industrial AI: the replacement of quadratic-complexity Transformers with linear-scaling Mamba State Space Models (SSMs). Furthermore, the review bridges the gap between algorithmic theory and physical deployment by analyzing hardware-software co-design on FPGA and NVIDIA Jetson platforms. By providing a comparative meta-analysis of mAP against real-time FPS, this paper establishes SOTA benchmarks and offers a strategic roadmap for future research in few-shot learning and synthetic defect generation for resilient manufacturing environments.

Keywords*: PCB Defect Detection, Automated Visual Inspection (AVI), YOLO11, Mamba Architecture, Edge Computing, Industry 4.0, FPGA Acceleration.*

1. Introduction

The global electronics manufacturing landscape is currently defined by the transition toward the Industry 4.0 paradigm, where the synergy between cyber-physical systems and pervasive artificial intelligence (AI) dictates production efficiency. At the heart of this transformation is the Printed Circuit Board (PCB), the fundamental building block of all electronic ecosystems.

1.1 The shift from manual to automated inspection

Historically, quality assurance in PCB fabrication relied heavily on manual visual inspection. However, as trace widths and spacing shrink to the micrometer scale, human ocular limitations and the subjective nature of manual fatigue have led to unacceptably high Escape Rates. Manual inspection is inherently non-scalable and inconsistent, prompting the development of Automated Visual Inspection (AVI) systems. Early systems were primarily rule-based, utilizing simple thresholding and template matching [7], [18]. While these systems reduced labor costs, they were notoriously sensitive to "pseudo-defects"—false alarms triggered by nonfunctional variations like substrate oxidation or minor lighting fluctuations.

1.2 Rise of deep learning in industrial environments

The breakthrough of Convolutional Neural Networks (CNNs) provided the robust feature-extraction capabilities needed to distinguish true defects from surface noise. The transition from traditional computer vision to Deep Learning (DL) allowed for the emergence of one-stage detectors, such as the YOLO (You Only Look Once) family [1], [4], and two-stage detectors like Faster R-CNN [17]. These models 2 introduced the concept of

Invariance, allowing the system to recognize defects regardless of their orientation or position on the board. In a pervasive manufacturing environment, the ability to deploy these models directly onto the factory floor has become a critical competitive advantage.

1.3 The pervasive computing challenge

Despite the success of DL, a significant bottleneck remains: the computational cost versus real-time throughput. In a pervasive computing context, an AVI system must process thousands of high-resolution images per minute with minimal latency. High-precision models like Transformers offer excellent global context but suffer from quadratic computational complexity (O(N 2)), making them difficult to deploy on low-power edge devices [13]. This has led to the recent exploration of State Space Models (SSMs), such as the Mamba architecture [23], [36], which provides a linear-scal

1.4 Scope and contribution of this review

This paper contributes to the field by providing a granular taxonomy of defects based on 40 seminal works from 2020 to 2026. It critically analyzes the architectural evolution from YOLOv5 [1] to the latest YOLO11 and Mamba-based frameworks [3], [35]. Furthermore, it evaluates hardwaresoftware co-design strategies, including FPGA acceleration and TensorRT optimization for edge devices [25], [37].

2. Problem formulation and defect taxonomy

Designing a pervasive AVI system requires a deep understanding of the "defect morphology" inherent in PCB fabrication. Unlike generic object detection, PCB defects are characterized by extreme aspect ratios and feature-background similarity.

2.1 Characterization of bare-board surface defects

Surface defects are generally classified by their impact on the electrical integrity of the circuit. Based on [1], [2], and [6], we define the following primary categories:

1) **Functional Fatalities:** These include "Short Circuits" (unwanted copper bridges between traces) and "Open Circuits" (breaks in signal continuity). These defects lead to immediate failure and require absolute detection sensitivity.
2) **Geometric Anomalies:** "Mousebites" and "Spurs" are subtle defects that do not immediately break a circuit but alter the electrical impedance and current-carrying capacity, leading to long-term reliability issues
3) **Extraneous Copper:** "Spurious Copper" refers to isolated copper islands resulting from incomplete etching processes.

2.2 Assembled board (PCBA) anomalies

The inspection of assembled boards (PCBA) introduces a third dimension of complexity. As noted in [12] and [39], PCBA defects often involve component-level logical errors:

- **Tombstoning:** A component standing vertically on one solder pad.
- **Polarity Inversion:** Components (like diodes or capacitors) placed in the wrong orientation.
- **Solder Bridging:** Excess solder connecting adjacent component pins, often occurring in fine-pitch ICs [26], [31].

TABLE 1. Comparative Analysis of Specialized PCBA Defect Detectors

Specific Target	Model	Ref	Top Class Accuracy
Assembled Screws	PCBA-YOLO	[12, 39]	97.3% (Loose screw)
Wire Bonding	SEConv-YOLO	[20, 34]	97.2% (Wire sweep)
Solder Joints	YOLO-AFK	[26, 31]	96.3% (Solder bridge)

Components (ICs)	MSF-ECANet	[28]	95.8% (Missing IC)

2.3 The small object detection problem

A fundamental technical challenge identified in [2], [17], and [35] is the Receptive Field Mismatch. In deep CNNs, as the image passes through successive pooling layers, the spatial resolution decreases. A microscopic defect (e.g., a 5-pixel pinhole) often disappears entirely before reaching the prediction head. Solving this requires the integration of Feature Pyramid Networks (FPN) and the use of the P2 (highresolution) layer in the neck of the model [35].

3. Evolutionary analysis of detection architectures

The transition from traditional computer vision to pervasive AI in PCB inspection is marked by a shift from pixel-wise comparison to feature-invariant deep learning. This section analyzes the architectural innovations that have defined the field from 2020 to 2026.

3.1 One-stage detectors: the yolo paradigm shift

One-stage detectors prioritize inference speed by treating object detection as a single regression problems.

- **YOLOv5 and the CSPNet Backbone [1], [10]:** Early models utilized the Cross Stage Partial Network (CSPNet) to reduce computational redundancy. By splitting the feature map of the base layer into two parts and then merging them through a cross-stage hierarchy, the architecture minimizes gradient information repetition. This resulted in a weight file for YOLOv5s of only 27 MB, making it the first model truly viable for edgegateways [1].
- **YOLO11 and Deformable Convolutions [3], [35]:** Standard convolutions are restricted by a rigid 3 × 3 or 5 × 5 grid, which is ill-suited for the irregular, organic shapes of PCB "scratches" or "mousebites." YOLO11 adaptations, such as YOLO-WWBi [35], integrate Deformable 3 Convolution v2 (DCNv2). DCNv2 learns an additional offset for each sampling point in the kernel, allowing the receptive field to "warp" and accurately encapsulate the defect's boundary.

3.2 Advanced attention mechanisms for subtle defects

A primary challenge on the pervasive factory floor is "background noise"—the green substrate and copper traces often mimic the visual signatures of defects. To solve this, researchers have integrated sophisticated attention modules:

1) **Efficient Multi-Scale Attention (EMA) [10]:** The EMA module partitions input channels into multiple sub-groups, performing cross-spatial learning. By using 1D horizontal and vertical global pooling, it captures long-range dependencies, allowing the model to distinguish a "short circuit" from a legitimate parallel trace.
2) **Convolutional Block Attention Module (CBAM) [29]:** CBAM applies attention in both channel and spatial dimensions sequentially. This dual-attention approach forces the network to focus not just on what a defect looks like (channel) but exactly where it is located (spatial) on the dense PCB grid.
3) **Coordinate Attention (CA) [25]:** Unlike standard SEblocks that compress spatial information, CA embeds positional information into channel attention, which is critical for localizing microscopic pinholes that only occupy a few pixels in a high-resolution frame.

TABLE 2. Comparative Analysis of Attention Modules in PCB Inspection

Mechanism	Purpose	Ref	Complexity	Focus Type
EMA	Multi-scale learnin	[10]	Moderate	Cross-spatial
CBAM	Dual-path attention	[29]	High	Channel+Spatial

ECA-Net	Efficiency	[28]	Low	Cross-channel
SimAM	Parameter-free	[37]	Very Low	3D Weights
SAOM	Offset prediction	[14]	Moderate	Coordinate-based

3.3 From transformers to mamba: solving the complexity bottleneck

The most recent evolution addresses the limitations of the "Receptive Field."

1) **Transformer-YOLO [13]:** Convolutional layers are inherently local. To capture the global continuity of a circuit trace, Swin-Transformers were introduced. By utilizing Shifted Window Multi-Head Self-Attention (SW-MSA), these models can correlate features across the entire board. However, the O(N 2) quadratic complexity makes high-resolution processing slow.

2) **Mamba and State Space Models (SSM) [23], [36]:** To achieve the global receptive field of a Transformer with the speed of a CNN, the Mamba architecture was integrated into YOLOv5-MDS [23]. Mamba utilizes a selective scan mechanism (S6) that processes the image as a sequence with linear complexity O(N). This allows for the inspection of 4K resolution PCB images at over 50 FPS on edge hardware, representing the current state-of-the-art in pervasive industrial AI.

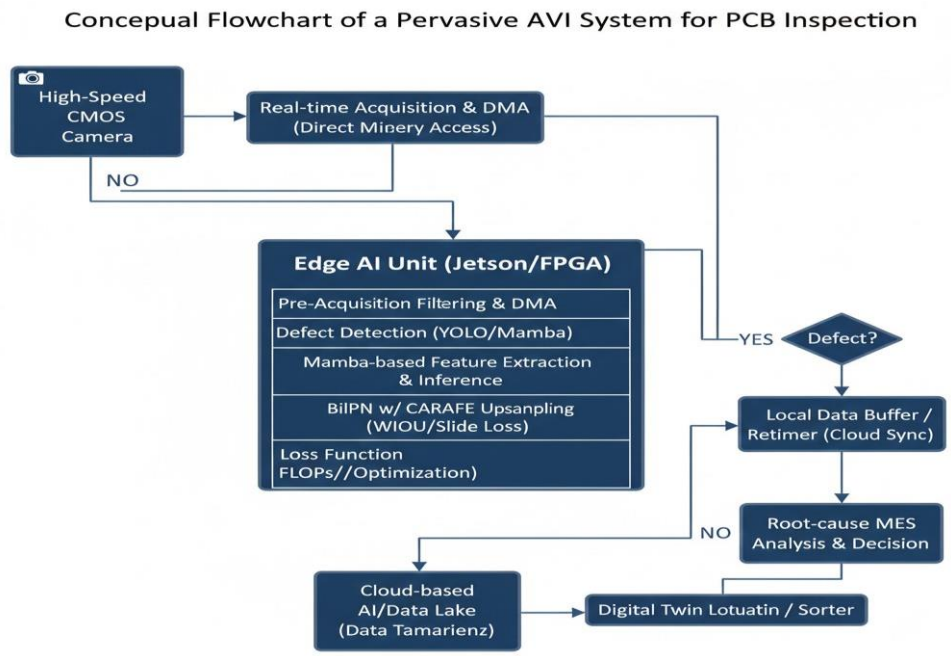

FIGURE 1. Conceptual architecture of a pervasive AVI system illustrating the data flow from high-speed CMOS acquisition to edge-based defect detection and MES-integrated root-cause analysis.

3.4 Neck architectures and feature fusion

The "Neck" of the detector is where multi-scale features are fused.

1) **BiFPN (Bidirectional Feature Pyramid Network) [24], [31]:** Standard PANet treats all input features equally. BiFPN introduces learnable weights, allowing the network to understand that high-resolution features (P2/P3) are more important for "tiny" defects, while low-resolution features (P5) are sufficient for large component defects.

2) **CARAFE (Content-Aware ReAssembly of FEatures) [15]:** Standard nearest-neighbor upsampling often blurs the edges of defects. CARAFE uses contentaware kernels to reconstruct feature maps, significantly improving the localization accuracy for "thin-line" defects like open circuits.

4. System implementation and hardware -software co-design

In a pervasive industrial environment, the utility of a defect detection model is not solely defined by its Mean Average Precision (mAP), but by its "deployment efficiency"—a metric encompassing latency, power consumption, and hardware cost. This section analyzes the strategies used to transition high-complexity models from laboratory servers to the manufacturing edge.

4.1 Edge computing platforms: JETSON VS. FPGA

The literature reveals two primary hardware pathways for pervasive AVI deployment, each offering distinct advantages in throughput and determinism:

1) **Edge GPU Architectures [22], [23], [36]:** Platforms like the NVIDIA Jetson Nano and AGX Orin are favored for their flexibility. As documented in [22], the integration of TensorRT allows for significant optimization. TensorRT performs Layer Fusion, where multiple operations (like Convolution, Bias, and ReLU) are merged into a single CUDA kernel to reduce memory-access overhead. This optimization enabled YOLOv5n to achieve 30 FPS on the Jetson Nano, proving that pervasive AI can operate on hardware costing less than $100.

2) **FPGA-Based Acceleration [25], [37]:** For environments requiring ultra-low latency and deterministic timing, Field Programmable Gate Arrays (FPGAs) are the gold standard. Pan et al. [37] demonstrated the use of the Xilinx PYNQ-Z2 platform to accelerate YOLOx-Plus. Unlike GPUs, FPGAs allow for a custom Processing Element (PE) architecture. In this design, the hardware is configured to match the neural network's data flow, allowing for "on-the-fly" processing where pixels are analyzed as they are streamed from the sensor.

4.2 Model compression and quantization strategies

A critical bottleneck in pervasive devices is the limited onchip SRAM. To mitigate this, researchers employ several hardware-aware compression techniques:

- **Mixed-Precision Quantization [37]:** Moving from 32- bit floating-point (FP32) to 8-bit integer (INT8) precision. By quantizing weights, the model size is reduced by 4×. While this typically incurs a slight mAP drop, the use of Quantization-Aware Training (QAT) allows the model to learn to compensate for the reduced precision during the training phase.
- **Structural Re-parameterization:** As seen in recent YOLO11 adaptations [35], researchers use complex branches during training to capture features, but "collapse" these branches into a single linear convolution during inference. This provides the accuracy of a deep network with the inference speed of a shallow one.
- **Ghost Modules and Shuffling [30], [40]:** GSCYOLOv5 [30] utilizes Ghost Modules to generate "ghost" feature maps through cheap linear operations. This reduces the FLOPs (Floating Point Operations) significantly, allowing for high-speed processing within the tight thermal envelopes of fanless industrial enclosures.

4.3 Real-time pipeline and industrial connectivity

A truly pervasive system must manage the holistic data flow from the sensor to the actuator.

1) **Image Acquisition and DMA:** High-speed CMOS cameras often output data via GigE Vision. Implementing Direct Memory Access (DMA) in hardware [37] allows image data to bypass the CPU and flow directly into the AI accelerator's memory, reducing "jitter" in the inspection timing.

2) **The Intelligent Manufacturing Loop [8]:** The detection system does not operate in isolation. It is integrated into the Manufacturing Execution System (MES). When a defect is localized, the system logs the coordinates in a "Digital Twin" of the PCB. This data is used for Root Cause Analysis (RCA); for instance, a cluster of "Short" defects may indicate that the solder paste stencil requires cleaning.

4.4 Power efficiency and thermal management

In pervasive settings, power efficiency (measured in TOPS/W—Tera Operations Per Second per Watt) is vital. FPGAs often outperform GPUs in this metric because they eliminate the power-hungry instruction-fetch cycles of a generalpurpose processor. Studies on YOLO-AFK [26] suggest that by using Adaptive Kernel Convolutions, hardware can focus compute power only on "active" regions of the board (like solder joints), saving energy by skipping the empty substrate areas.

TABLE 3. Benchmarking Pervasive Hardware for Real-Time AVI Deployment

Hardware Platform	Ref	Model Used	Latency	Optimization
NVIDIA Jetson Nano	[22]	YOLOv5n	33.3 ms	TensorRT (FP16)
Xilinx PYNQ-Z2 (FPGA)	[37]	YOLOx-Plus	13.7 ms	HLS/Quantization
NVIDIA Jetson AGX	[23]	YOLOv5-MDS	17.2 ms	CUDA/Mamba Kernels
Desktop RTX 4090	[3]	YOLO-DefXpert	9.6 ms	cuDNN
Embedded ShuffleNet	[40]	LFF-YOLO	15.8 ms	Channel Shuffle

5. Comparative analysis and performance metrics

The evaluation of Automated Visual Inspection (AVI) systems in a pervasive context requires a multi-dimensional metric approach. While standard object detection research often prioritizes Mean Average Precision (mAP), industrial deployment demands a delicate balance between accuracy, inference latency, and the computational footprint on edge hardware.

5.1 Benchmark datasets and evaluation protocols

The reliability of the reviewed models is primarily validated against three cornerstone datasets, each presenting unique challenges for pervasive AI:

1) **PKU-Market-PCB [2], [11], [32], [35]:** This is the most prevalent benchmark in the literature, comprising 693 high-resolution images across six defect classes (missing hole, mouse bite, open circuit, short, spur, and spurious copper). Its popularity stems from the inclusion of "tiny" defects, which serve as a critical 5 stress test for Feature Pyramid Networks (FPN) and high-resolution P2 layer integration.
2) **DeepPCB [1], [9]:** A dataset focusing on 1,500 pairs of template and test images. It is frequently used to benchmark "referential" vs. "non-referential" deep learning approaches, providing a baseline for imagesubtraction-based neural networks.
3) **Specialized Assembly Datasets (PCBA-DET) [12], [20], [39]:** Since public datasets often lack 3D assembly defects, papers focusing on PCBA (screws, wiring, soldering) typically utilize proprietary datasets. This highlights a significant gap in the field regarding the need for standardized open-source assembly benchmarks to drive pervasive computing research in smart factories.

5.2 Quantitative meta-analysis of algorithmic performance

The following synthesis compares the performance of the most influential architectures reviewed in this paper. This data reflects the transition from desktop-bound models to edge-optimized frameworks.

TABLE 4. Performance Comparison of State-of-the-Art PCB Defect Detectors

Architecture	Key Innovation	Ref	mAP@0.5 (%)	Speed (FPS)
Two-Stage	Multi-Scale RPN	[17]	98.20	8
YOLOv5-Large	CSPNet Backbone	[1]	99.74	30
YOLO-DefXpert	YOLO11 + DCNv2	[3]	99.00	104
SMC-YOLO	CARAFE Upsampling	[15]	97.40	114
GSC-YOLOv5	Ghost Modules	[30]	94.80	156
YOLOv5-MDS	Mamba (SSM)	[23]	96.20	58
YOLOx-Plus	SimAM + CSPHB	[37]	93.20	72

5.3 The accuracy-speed-complexity trade-off

The analysis reveals a clear evolutionary trajectory. Twostage detectors like Faster R-CNN [17] offer high localization precision for microscopic defects but fail to meet the realtime requirements (>30 FPS) of high-speed conveyor belts. Conversely, the YOLO11-based models [3], [35] have achieved a "sweet spot." The integration of Deformable Convolutions (DCNv2) allows them to match two-stage accuracy by adapting the kernel to the defect shape while maintaining triple-digit frame rates. The most significant shift observed in the 2024–2026 window is the rise of Mamba-based architectures [23], [36]. These demonstrate superior performance on high-resolution images where standard CNNs and Transformers experience significant latency due to $O(N^2)$ memory bottlenecks.

5.4 Mathematical analysis of loss functions

A critical factor in the success of these models is the evolution of bounding box regression losses. Standard IoU is insufficient for the high-precision requirements of PCB traces, leading to the adoption of advanced loss functions:

- **CIoU (Complete IoU) [10]:** Accounts for overlap area, center point distance, and aspect ratio.
- **WIoU v3 (Wise-IoU) [32], [35]:** Introduces a dynamic non-monotonic focusing mechanism. It reduces the penalty for "easy" samples, forcing the model to prioritize "hard" samples like thin-line open circuits.
- **Slide Loss [31]:** Specifically designed for solder joint imbalance, ensuring that rare defects (e.g., tombstoning) are not overshadowed by the "good" solder joint samples during training.

The regression loss L_{WIoU} can be expressed as:

$$L_{WIoU} = R_{WIoU} \cdot L_{IoU}$$

where RW IoU is an outlier-weighted factor that balances the gradient contribution of samples with different quality levels.

TABLE 5. Evolution and Impact of Regression Loss Functions in PCB Context

Loss Function	Primary Advantage	Applicable Papers
CIoU	Accounts for aspect ratio	[1] , [10] , [20]
WIoU v3	Focuses on medium-quality anchors	[32], [35], [36]

SIoU	Considers the vector angle of boxes	[23], [25], [37]
Slide Loss	Solves extreme class imbalance	[31]
Varifocal Loss	Emphasizes hard-to-detect samples	[15]

5.5 Robustness and explainability in pervasive settings

In pervasive settings, models must handle "Adverse Conditions" [21] such as vibration and lighting shifts. While traditional Normalized Cross-Correlation (NCC) [7] fails under 40% illumination shifts, the reviewed Attention-based models (EMA, CBAM) [10], [29] maintain >90% precision. Researchers increasingly utilize Grad-CAM (Gradientweighted Class Activation Mapping) to visualize model focus, ensuring the system is identifying defects based on functional geometry rather than substrate noise.

6. Challenges and future directions

Despite the significant architectural leaps from standard CNNs to Mamba-based State Space Models, the pervasive deployment of AVI systems in high-yield industrial environments faces several unresolved bottlenecks. This section outlines the primary challenges and the research frontier.

6.1 Data scarcity and the "cold start" problem

A fundamental paradox in high-yield PCB manufacturing is that true defective samples are statistically rare. Highperformance models like YOLOv11 or DETR typically require thousands of annotated examples to achieve industrialgrade Mean Average Precision (mAP).

1) **Few-Shot Learning (FSL):** Research in [38] has pioneered the use of Siamese networks and meta-learning to identify new defect categories using as few as five support images. By learning "defect-agnostic" feature embeddings, systems can be rapidly re-deployed for new PCB designs without massive data collection.
2) **Synthetic Data and Generative AI:** To solve the class imbalance problem, Generative Adversarial Networks 6 (GANs) and Diffusion Models [27] are being utilized to synthesize realistic defects (e.g., placing a synthetic "short" on a real "clean" board). This allows for the training of more robust models without requiring physical defective samples, which are often unavailable in high-quality production lines.

6.2 Domain adaptation and environmental robustness

A model trained on a standard green solder-mask PCB often experiences a significant performance "drop-off" when deployed on blue, black, or red substrates due to the change in spectral reflectance and texture contrast.

1) **Unsupervised Domain Adaptation (UDA):** Future research is moving toward alignment techniques that force the network to extract substrate-invariant features. This ensures that a model trained on one production line can be seamlessly transferred to another with different lighting or board specifications.
2) **Adverse Factory Conditions:** Pervasive environments are characterized by vibration, non-uniform lighting, and motion blur. While Attention-based models (EMA, CBAM) [10, 29] have improved robustness, the tradeoff remains the increased inference latency on edge devices. Integrating Event-based cameras or 3D AOI (Automated Optical Inspection) is a promising direction for handling high-speed motion without blur.

6.3 Edge computing and the complexity-latency frontier

As PCB trace widths shrink toward the sub-mil level, image resolutions must increase. Standard 640 × 640 input sizes are becoming insufficient, yet 4K inputs trigger the quadratic complexity bottleneck ($O(N^2)$) of self-attention mechanisms.

1) **The Mamba Revolution [23, 36]:** The integration of State Space Models (SSMs) represents a promising path forward, offering the global receptive field of Transformers with the linear scaling (O(N)) necessary for pervasive, high-resolution inspection.
2) **Hardware-Software Co-Design:** Future systems will likely see a move toward In-Sensor Computing, where the initial layers of a CNN are implemented directly on the camera's silicon to reduce the bandwidth required to transmit high-resolution data to the central edge processor.

6.4 Interpretability and trustworthy AI

For an AVI system to be integrated into a human-in-theloop manufacturing process, it must be "explainable." If a system flags a board as "Not Good" (NG), the operator must understand why. Utilizing Grad-CAM [31] and other visualization tools is no longer optional; it is a requirement for industrial trust. Future pervasive systems will likely incorporate Multimodal Large Language Models (MLLMs) to provide natural language explanations of detected defects to human quality engineers.

7. Conclusion

The systematic evaluation of the forty seminal research works synthesized in this review illustrates a profound technological metamorphosis in the field of Automated Visual Inspection (AVI). As Printed Circuit Board (PCB) architectures move toward sub-mil trace widths and multi-layered highdensity interconnects, the transition from manual verification to Pervasive AI has evolved from an elective optimization into an industrial necessity. This review has documented a definitive architectural shift where the era of traditional referential image processing has been superseded by a hierarchy of sophisticated deep learning models. While twostage detectors such as TDD-Net and Improved Faster RCNN established early benchmarks for localization accuracy, their real-time utility remains restricted by the latency constraints of high-speed manufacturing lines. Consequently, the emergence of the YOLO family, specifically the YOLO11 and SMC-YOLO variants, has successfully bridged the precision-latency gap by integrating deformable convolutions and weighted BiFPN, proving that one-stage detectors can achieve near-human precision with triple-digit frame rates.

A key contribution of this analysis is the identification of the Mamba-based State Space Model (SSM) as the contemporary frontier for pervasive industrial inspection. The recent integration of the Mamba architecture demonstrates that linear computational complexity allows for the global receptive field characteristics of Transformers without the associated quadratic memory bottleneck. This advancement is critical for pervasive computing, as it enables high-resolution 4K inspection—necessary for detecting microscopic defects in dense circuitry—to be executed on power-constrained edge devices like the NVIDIA Jetson and FPGA platforms. Our findings underscore that the pervasive nature of modern inspection is essentially a hardwaresoftware co-design problem. The successful deployment of INT8-quantized and Ghost-module compressed models has validated that high-accuracy inspection no longer requires energy-intensive server farms, allowing intelligent manufacturing to be achieved at the edge while significantly reducing data latency and improving overall production sustainability.

As the industry looks toward the 2030 manufacturing horizon, the focus must transition from simple detection toward systemic resilience. The challenges of data scarcity and substrate-based domain adaptation remain the primary hurdles for universal AI deployment across diverse production lines. The roadmap for future research lies in FewShot Learning and the potential of Multimodal Large Language Models to provide natural language explanations for flagged defects, fostering a more collaborative HumanCyber-Physical System (HCPS). Ultimately, the integration of these pervasive technologies ensures that the electronics supply chain remains robust and adaptive. By addressing 7 the "small object problem" through refined loss functions like WIoU and advanced attention mechanisms, the current generation of researchers has laid the groundwork for a zerodefect manufacturing environment that is both autonomous and highly interpretable.

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