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Low Power Wallace Multiplier Using Gate Diffusion Input Based Full Adders

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***Abstract*:** Now a days, in CMOS circuits leakage power is becoming more and more remarkable in power dissipation. Digital signal processing performs many functions including multiplication which is the prominent one. In the design of energy efficient processor multipliers play a key role in which it determines the DSP processor efficiency. A 4*4Wallace tree multiplier employs gate diffusion input technique to minimize leakage power. It is designed by adopting one bit full adder. In the proposed method, full addersare replaced by4*4 Wallace tree multiplier. Power dissipation majorly occurs in full adders. Hence, minimizing power dissipation in full adders will shrink dissipation of power in multipliers. Here, the proposed work diminishes the leakage power in comparison with the existing method.

Krywords *: existing, efficiency, designed, processing*

1. Introduction

Digital signal processing applications employs multipliers to perform arithmetic operations. Now a days, processors are designed in achieving low power architecture adopted in their circuit. Hence, necessity of low power multipliers is becoming more and more. For understanding high speed technologies, many kinds of low power multipliers are fabricated. Design of low power techniques are essential to keep away from increase of chip area or surrender the speed of the system.

Wallace tree multiplier consists of three roots of power dissipation. First one is the logic transitions where the nodes in CMOS circuit shifts between the 0 and 1, the free capacitances charges and discharges continuously. Transistor resistances permits the current flow and this energy is transferred as heat which is dissipated outside. Disspation of power element is proportional to voltage supply, mean capacitance per cycle and voltage changes along the node. Dissipaton of power because of shifting continuously from 0 to 1 or 1 to 0 is the voltage supply that is squared.

Second way of dissipation of power is due to Short-circuit currents which travels from supply to ground that is when both Pull-Up Network and Pull-Down Network conduct at once. Out of the two inputs to gate stability, one network conducts and there is no flow of current in the short-circuit. But output at the gate changes to the change in inputs which reflects PUD and PDN to conduct for a short time period. Thus, Static power dissipation came into the picture which is the final source of dissipation of power.

Leakage current is very low and was neglected in the past few decades. In recent days, dynamic power is decremented due to scaling of supply voltage and also MOSFETs with Vth are used. Vth scaling results in sub- threshold leakage current to increase exponentially. It is the leakage current from drain-to-source during the transistor logic is low. It occurs when Vgs < threshold Vth.Now, Current is due to minority carriers of MOSFET.

Leakage power in 4*4 Wallace tree multiplier is minimized by employing gate diffusion input technique. The main objective of this work is to minimize dissipation of power in Wallace tree multiplier by employing gate diffusion input technique based full adders in place of all full adders.

2. Existing method

Here, we will elaborate about various techniques employed in 4*4 Wallace tree multiplie to decrease leakage power. This leakage power is due to dissipation from short circuit as well as dynamic and static. So, we should decrease one of them to reduce leakage power. There are different techniques that are proposed for Wallace tree multiplier to decrement the leakage power. C.S.Wallace, a scientist in 1960's proposed fast multiplier which integrates half adders and full adders. In those periods, low power designs are not developed, but now a days we require improved techniques with delay, speed, low power dissipation in the new designs. Therefore, multiplier circuits are designed to satify the above needs. Also, research have been improved in developing these circuits.

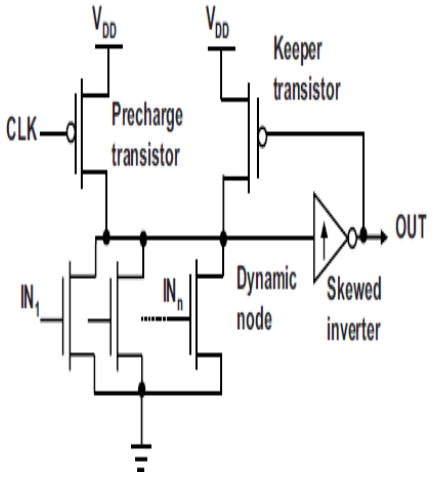

Fig 1: Schematic representation of standard domino logic

Wallace multiplier including full adder technique improves in decreasing dissipation of leakage power. There are some famous techniques which are employed to decrease dissipation of static power are discussed as follows; input vector method which depends on input vector to gate. In the idle state we employ control logic to get low leakage and come back to the initial state. Also, it needs specific latches to get back to the initial state which increases the area of the chip five times.

Power-gating is an another method for controlling leakage power. In this method, supply voltage is in open condition to switch-off the components. However, large sleeping transistors like PMOS or NMOS components are included in the middle of supply and circuit or ground and circuit. These transistors develop virtual power as well as ground in the design. Circuit is in the idle when the transistors are in OFF state and transistors are ON when circuit is active. It is occurred by employing sleep signals. Since Vth changes exponentially with leakage power, there is a need for the transistors having high voltage. Hence, we go for employing multiple threshold voltage CMOS. Douseki a scientist, developed Multi- Threshold CMOS (MTCMOS) that is considered to be a famous method to reduce leakage power. In NMOS transistor ,Logic gates along with transistors are low threshold circuits whereas high threshold voltage is connected with ground. Gating transistor is considered to be a sleep transistor. It results in decrease noise margin due to the presence of conducting routes.

The modified MTCMOS technique is a Dual Vth method which employs sleep transistors having varying voltages. Gates in specific paths are employed with Low threshold transistors whereas Gates in non specific paths are employed with high threshold transistors.

Domino logic techniques may decrease dynamic power dissipations. Below figure shows a standard domino circuit. So, employing standard domino logic circuit a multiplier circuit is developed.

PMOS keeper transistor is the one which is employs to limit unacceptable discharging at the circuit node for the purpose of leakage currents. Also, in evaluation phase there occurs sharing of charges in pull-down networks. Therefore, it develops robustness of the circuit. Also, conventional keeper approach which is less productive in present day CMOS technology. The upsizing of keeper develops noise immunity and increments consumption of power. Hence, this technique, increments consumption of power and delay of the above discussed circuits.

Conditional keeper domino logic style is a different technique which varies the gate voltage of controlling circuit that is shown in figure.

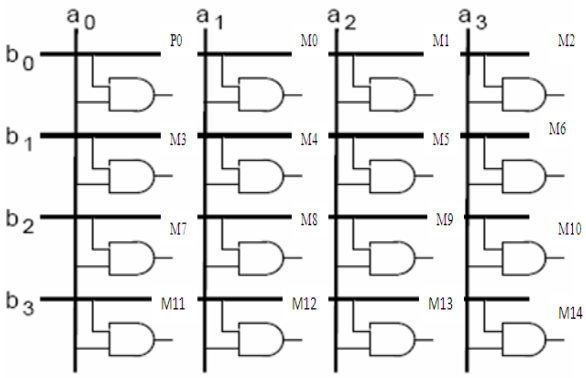

Fig 2: Schematic representation of Conditional keeper domino logic

In the design a multiplier, if the above this logic design is employed then the leakage current increases. High speed domino is another technique employed to decrease leakage power is observed in below figure. Here, leakage power is more because of the variation in gate voltage of the controlling circuit.

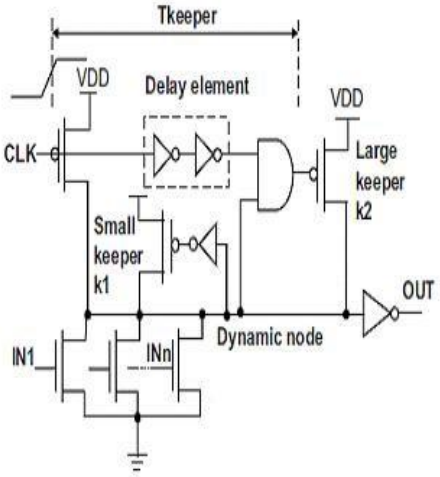

Fig 3: Schematic representation of High speed domino logic

3. Proposed Work

In this case, full adders are replaced by half adders and then by 4*4 Wallace tree multiplier with full adder. Figure 4,5 says no separate summing system is required. Hence, we get low leakage power.

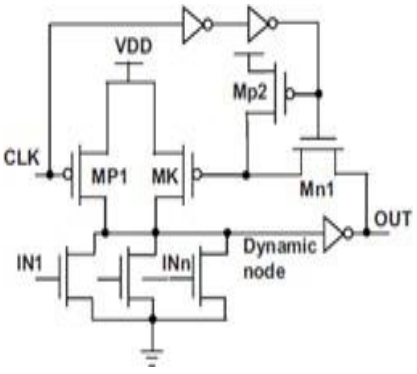

Fig 4: Schematic representation of AND gate producing multiplier

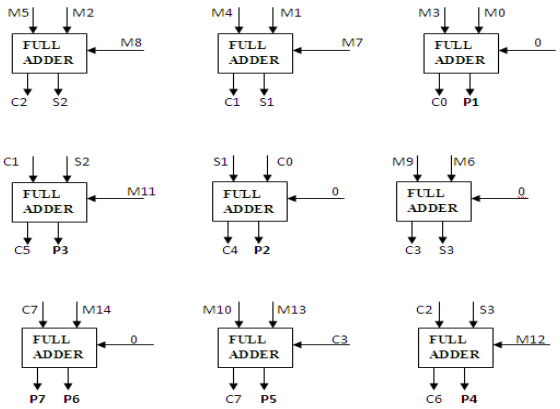

Fig 5: Schematic representation of full adder based Multiplier

The above mentioned is the principle approach in reducing leakage power. Also, gate diffusion input technique based full adders are placed in full adders of 4*4 Wallace tree multiplier. Employing the above technique, various kinds of full adders are developed. These types consists of 10 transistors to produce carry and sum each time.

3.1 Basic Gate Diffusion Input Technique

The Simple cell dependent Gate Diffusion Input method is observed in above figure.

1.There are three inputs in Gate Diffusion method which are namely P,N, common gate input of NMOS and PMOS.

2. NMOS,PMOS are attached to Nor P. So, they are opposite to CMOS inverter.

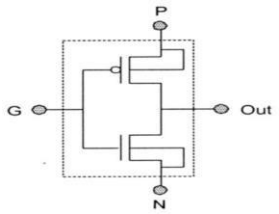

Fig 6: Schematic representation of Gate diffusion input basic cell(GDI)

It confirms that all the functions are not happened in p-well CMOS. It is adopted successfully in silicon on insulator (SOI) technologies. The below table comes to a conclusion that small variation of simple GDI links to various arithmetic functions. These functions are tedious in CMOS and PTL but simple in GDI. The proposed work is based on F1, F2 functions respectively.

1. F1,F2 permits realization of all logic functions with two input set.
2. F1, only Gate Diffusion Input function that is realized in p-well CMOS.
3. There occurs a short between N and P due to N input high logic and P input low logic helps in dissipation of power in the static mode.

Table 1: Representation of logical functions of gate diffusion input cell

N	P	G	OUT	FUNCTION
0	B	A	A’B	F1
0	1	A	A’+B	F2

1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

3.2 Logic equation for the proposed full adder

The following are the operations of full adder in which A, B and C are the three inputs which produce sum carry the two outputs.

Sum = A XOR B XOR C_{in}

Sum = A XNOR B XNOR C_{in}

Sum = C'_{in} (A XOR B)+ C_{in} (A XNOR B)

Carry =A(A XNOR B)+ C'_{in} (A XOR B)

3.3 XOR and XNOR gates based on Gate Diffusion Input cell

Gate diffusion Input cells will depend on XOR, XNOR gates are the basic applications. Below figure shows that each circuit requires four transistors. So, we can say that Gate diffusion Input XOR and XNOR gates employs less number of transistors in comparison with traditional CMOS circuits.

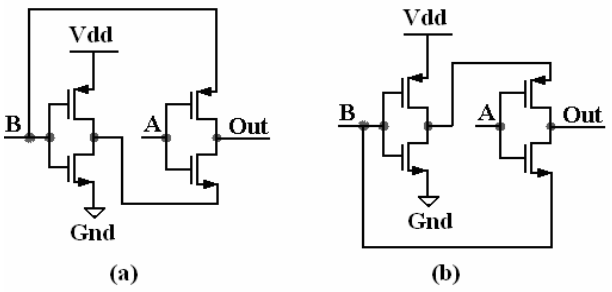

Fig 7: (a) Schematic representation of GDI XOR gate ,(b) Schematic representation of GDI XNOR gate

Based on the equations above and Gate diffusion Input XOR and XNOR gates technique, we can design two full adders which consists of 10 transistors. They are

1. Gate diffusion Input XOR full adder
2. Gate diffusion Input XNOR full adder

3.4 Gate Diffusion Input XOR full adder

Gate diffusion Input XOR full adder design is observed in below figure which contains three components. One is a multiplexer and the other two are Gate diffusion Input XOR gates. Sum and carry are evaluated first and last equations. Sum has 4-T delay whereas C_{out} has 3-T delay in the worst scenario. Still advantage of Gate diffusion Input cell helps in resulting consumption of low power.

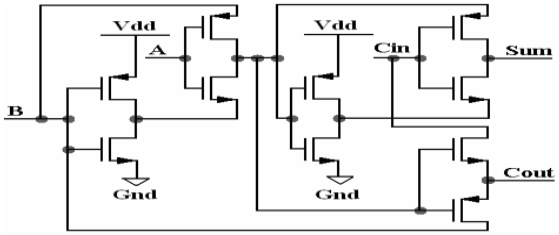

Fig 8: Schematic representation of GDI XOR full adder

3.5 Gate Diffusion Input XNOR full adder

Gate diffusion Input XNOR full adder observed in below figure is a standard application. It also contains three components. One is a multiplexer and the other two are Gate diffusion Input XOR gates. Sum and carry are evaluated second and third equations. Sum has 4-T delay whereas C_{out} has 3-T delay in the worst scenario.

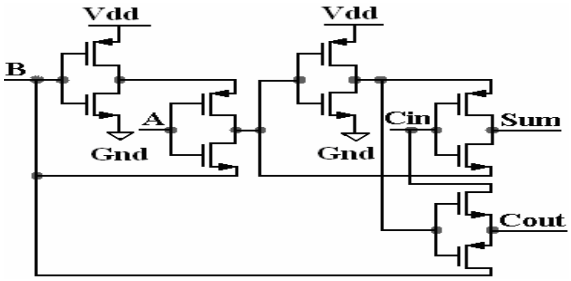

Fig 9: GDI XNOR full adder

If 4*4 Wallace tree multiplier is implemented by employing Gate diffusion Input XOR and XNOR full adders, count of transistors adopted is decremented. Due to this the switching activities of the transistors were reduced. Hence, dissipation of dynamic power decremented in 4*4 Wallace tree multiplier . Once CMOS VLSI circuits are designed at deep submicron technology the static power dissipation is degraded in comparison dynamic power dissipation. Hence, in many techniques leakage power dissipation is approximate to dynamic power dissipation.

4. Result

Here, two 4*4 Wallace tree multiplier with gate diffusion input full adders was designed which is simulated by using Tanner tool. In the first design the 4*4 Wallace tree multiplier used gate diffusion input XOR based full adder and in the second design the 4*4 Wallace tree multiplier used gate diffusion input XNOR based full adder. The simulation results from EDA Tanner tool are shown in Table 2. From the below Table 2 it is shown that the 4*4 multiplier with gate diffusion input XNOR based full adder has very less dynamic power dissipation in comparison with 4*4 Wallace tree multiplier with different logic based full adders.

Table 2: Representation of Comparison analysis of Wallace multiplier with different logic style full adders

4*4 WALLACE MULTIPLIER	DYNAMIC POWER DISSIPATION	DELAY	NUMBER OF TRANSISTORS
With Gate diffusion input XOR based full adders	$2.43*10^{-4}$W	2.2ns	296
With Gate diffusion input XNOR based full adders	$7.868*10^{-5}$W	1.38ns	288
With CMOS	$2.12*10^{-4}$W	1.2ns	320

based full adders			

5. Conclusion

The above Table 2, it shows that gate diffusion input XNOR dependent on 4*4 Wallace tree multiplier with full adder design has less delay, minimum transistors and less dissipation of dynamic power. When Wallace tree multiplier is designed in deep micron CMOS technology the static power dissipation is very less when compared to its counterpart dynamic power dissipation. So, dissipation of dynamic power contribute more to the total leakage power. By reducing dynamic power dissipation the final leakage power of 4*4 Wallace tree multiplier was reduced.

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